

# MileSan

Detecting Exploitable Microarchitectural Leakage via  
Differential Hardware-Software Taint Tracking

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Presented at CCS'25

ETH Zurich, \*UC Berkeley

**COMSE**C

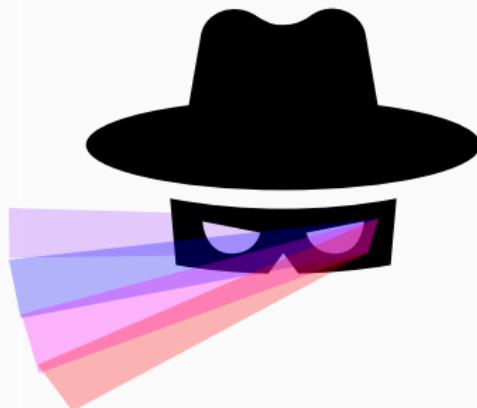
**ETH**zürich

# MileSan



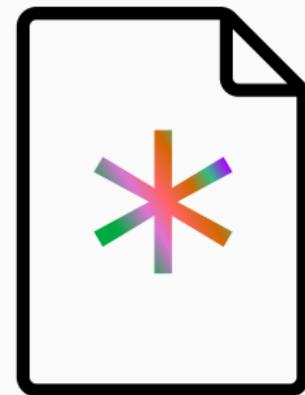
detects arbitrary  
exploitable leakage in RTL

## MileSan



detects arbitrary  
exploitable leakage in RTL

## RandOS



generates random  
operating systems

# MileS

# andOS



detects arb.  
exploitable leakage

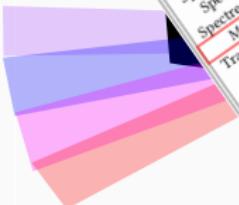
Vulnerability	DUT	Covert Channel	Previously found by	CVE
Spectre-V1	BOOM	DCACHE	[14, 23, 38] [23]	/
Spectre-V1-TLB	BOOM	TLB	[14, 23, 38]	/
Spectre-V2	BOOM	TLB	/	requested
Spectre-V2-TLB	BOOM	DCACHE	[14, 23]	requested
Spectre-V4	BOOM	TLB	/	/
Spectre-V4-TLB	BOOM	DCACHE	[14, 23]	requested
Spectre-RSB	BOOM	TLB	/	/
Spectre-RSB-TLB	BOOM	TLB	[14, 23]	CVE-2025-29343
Meltdown	BOOM	TLB	/	requested
Trans. Meltdown	BOOM	TLB	[14, 17, 23]	/
cp. Spectre V2	BOOM	TLB	/	CVE-2025-29340
MDS*	TLB	TLB	/	CVE-2025-29340
Spectre SLS	CVA6	TLB	/	CVE-2025-46004
cp Spectre-SLS	CVA6	TLB	/	CVE-2025-46004
MDS	CVA6	TLB	/	CVE-2025-46004
Trans. MDS	CVA6	TLB	/	CVE-2025-46004
div <sup>+</sup>	CVA6	DIV	[20]	/
divu <sup>+</sup>	CVA6	DIV	[20]	/
divw <sup>+</sup>	CVA6	DIV	[20]	/
rem <sup>+</sup>	CVA6	DIV	[20]	/
remu <sup>+</sup>	CVA6	DIV	[20]	/
remw <sup>+</sup>	CVA6	DIV	[20]	/
Spectre-V1	OpenC910	DCACHE	/	requested
Spectre-V1-TLB	OpenC910	TLB	/	requested
div <sup>+</sup>	OpenC910	DIV	/	CVE-2025-46005
divu <sup>+</sup>	OpenC910	DIV	/	CVE-2025-46005
divw <sup>+</sup>	OpenC910	DIV	/	CVE-2025-46005
rem <sup>+</sup>	OpenC910	DIV	/	CVE-2025-46005
remu <sup>+</sup>	OpenC910	DIV	/	CVE-2025-46005
remw <sup>+</sup>	OpenC910	DIV	/	CVE-2025-46005
random	OpenC910	DIV	/	CVE-2025-46005
ating systems	OpenC910	DIV	/	CVE-2025-46005

# Miles and OS

detects arbitrary exploitable leakage ~ random operating systems

# MileS

# andOS



detects arb.  
exploitable leakage

Vulnerability	DUT	Covert Channel	Previously found by	CVE
Spectre-V1	BOOM	DCACHE	[14, 23, 38] [23]	/
Spectre-V2	BOOM	TLB	[14, 23, 38]	requested
Spectre-V2-TLB	BOOM	TLB	/	requested
Spectre-V4	BOOM	DCACHE	[14, 23]	/
Spectre-V4-TLB	BOOM	TLB	[14, 23]	requested
Spectre-RSB	BOOM	DCACHE	/	CVE-2025-29343
Spectre-RSB-TLB	BOOM	TLB	[14, 23]	requested
Meltdown	BOOM	TLB	/	CVE-2025-29340
Trans. Meltdown	BOOM	TLB	/	CVE-2025-29340
cp. Spectre V2	BOOM	TLB	[14] <sup>2</sup>	CVE-2025-46004
MDS <sup>+</sup>	CVA6	TLB	/	CVE-2025-46004
Spectre SLS	CVA6	TLB	/	CVE-2025-46004
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div <sup>+</sup>	CVA6	DIV	[20]	requested
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div <sup>+</sup>	CVA6	DIV	[20]	CVE-2025-46005
divu <sup>+</sup>	CVA6	DIV	[20]	CVE-2025-46005
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Spectre-V1	OpenC910	DCACHE	/	CVE-2025-46005
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div <sup>+</sup>	OpenC910	DIV	[20]	CVE-2025-46005
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remu <sup>+</sup>	OpenC910	DIV	[20]	CVE-2025-46005

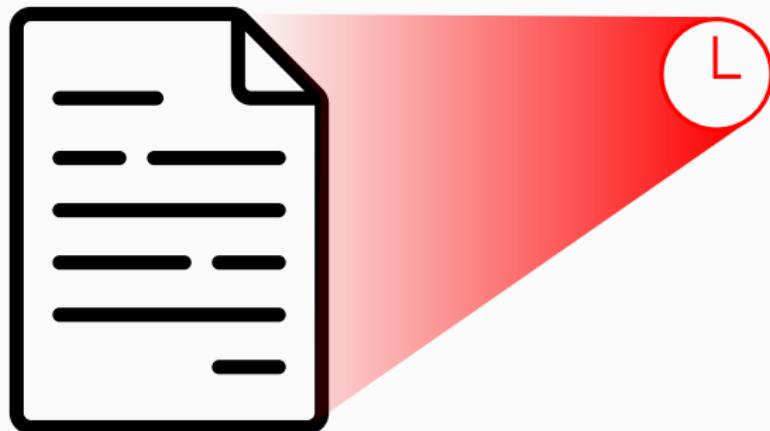
random  
targeting systems

Miles - Expert Channel / [14, 23] / [14, 23] / request / 0225-29343 - andOS

detects arbitrary exploitable leakage ~ random operating systems

**Problem.** Existing pre-silicon microarchitectural fuzzers overfit to known vulnerabilities.

# Overfitting in software for triggering leakage



# Overfitting in software for triggering leakage



# Overfitting in software for triggering leakage



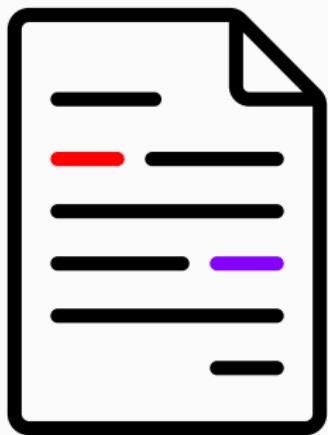
# Overfitting in software for triggering leakage



TRAINING\_GADGET



# Overfitting in software for triggering leakage

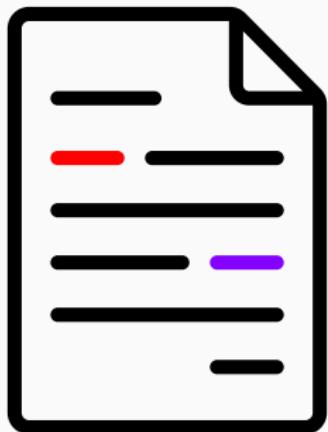


TRAINING\_GADGET

LEAKING\_GADGET



# Overfitting in software for triggering leakage

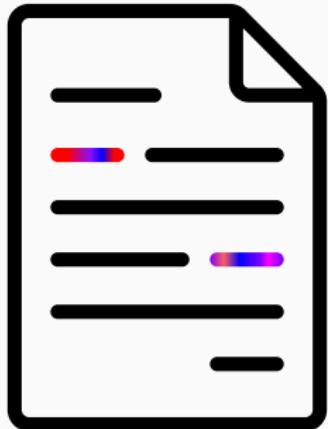


TRAINING\_GADGET

LEAKING\_GADGET



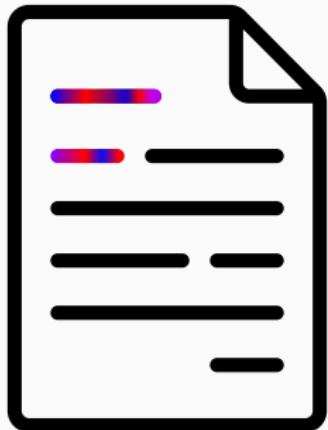
# Overfitting in software for triggering leakage



TRAINING\_GADGET

LEAKING\_GADGET

# Overfitting in software for triggering leakage



TRAINING\_GADGET

LEAKING\_GADGET

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TRAINING\_GADGET

LEAKING\_GADGET

# Overfitting in software for triggering leakage



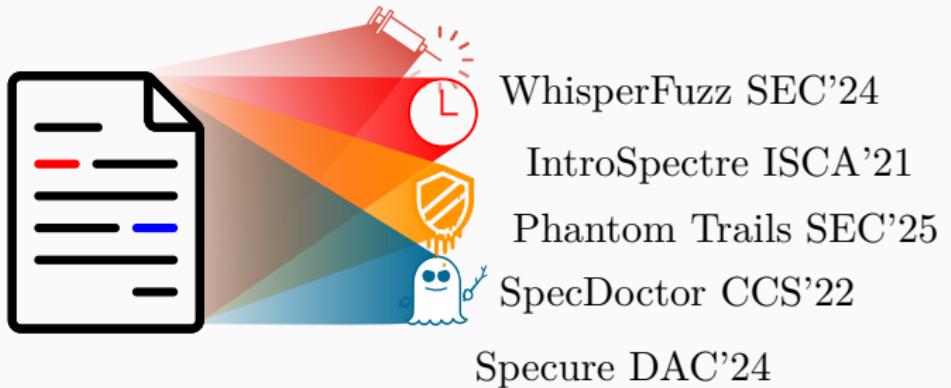
TRAINING\_GADGET

LEAKING\_GADGET

# Overfitting in software for triggering leakage



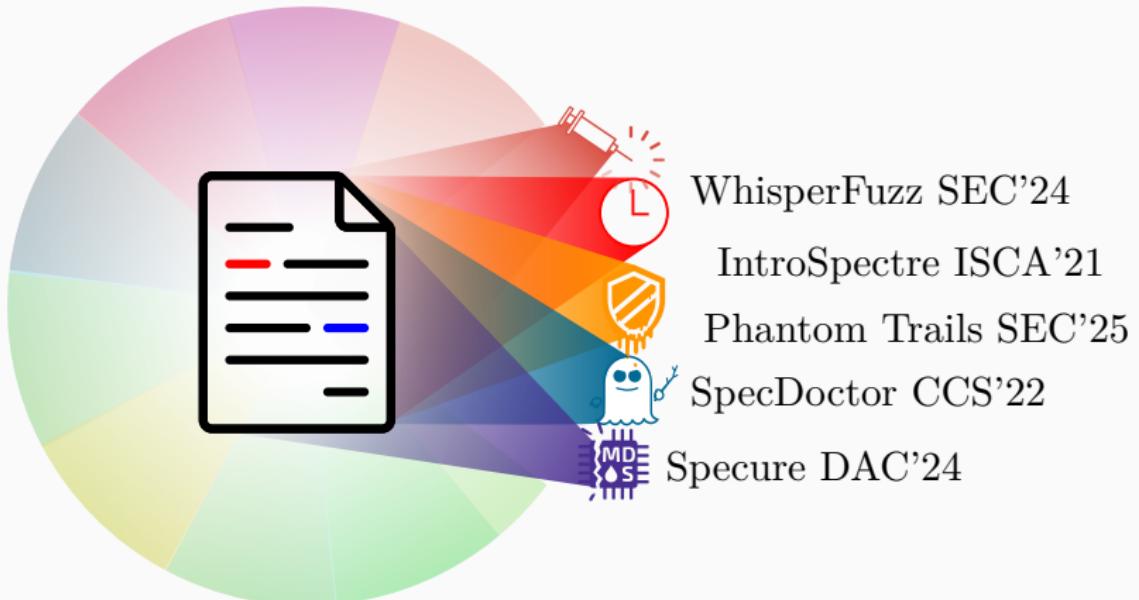
# Overfitting in software for triggering leakage



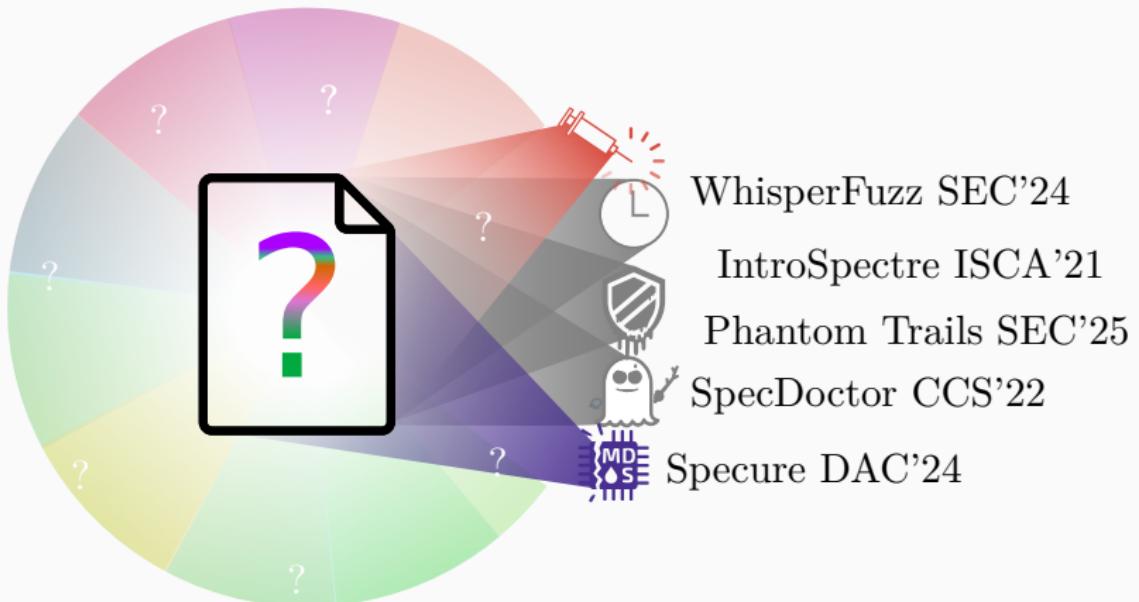
# Overfitting in software for triggering leakage



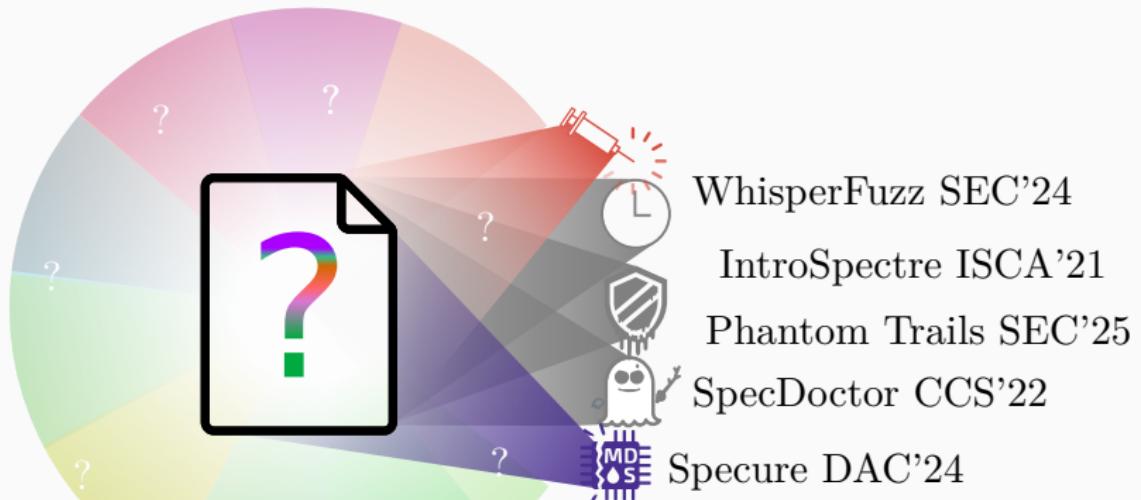
# Overfitting in software for triggering leakage



# Overfitting in software for triggering leakage

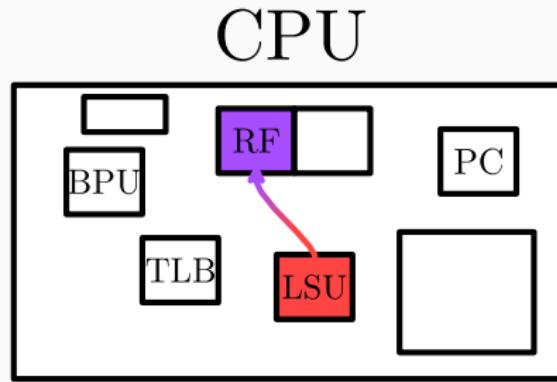


# Overfitting in software for triggering leakage

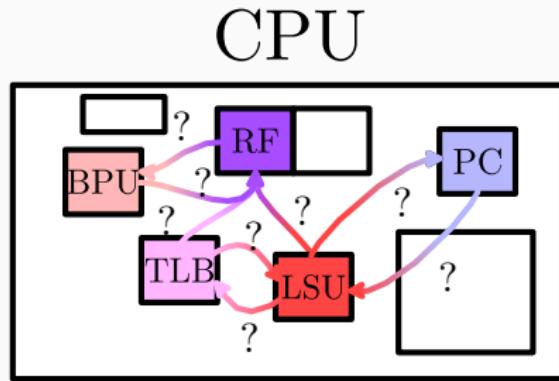


**Obs. 1.** Test case generation overfits to known vulnerabilities.

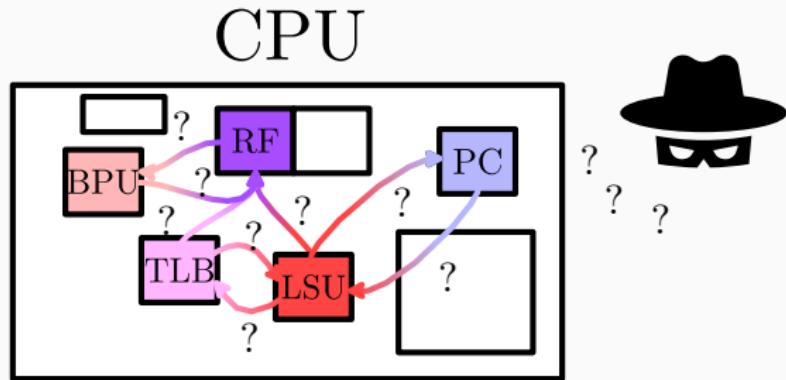
# Overfitting in hardware for detecting leakage



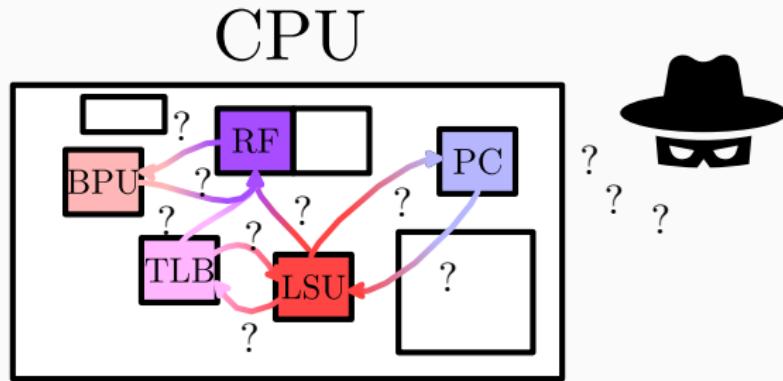
# Overfitting in hardware for detecting leakage



# Overfitting in hardware for detecting leakage



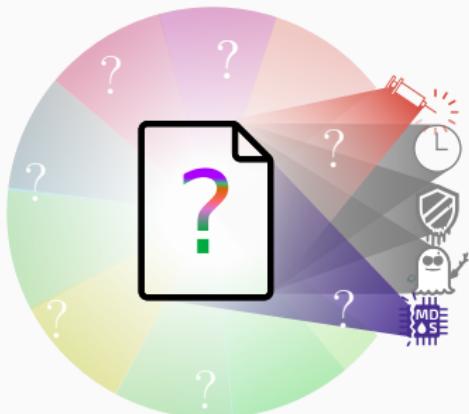
# Overfitting in hardware for detecting leakage



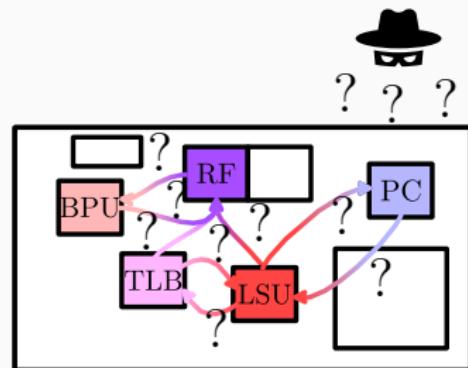
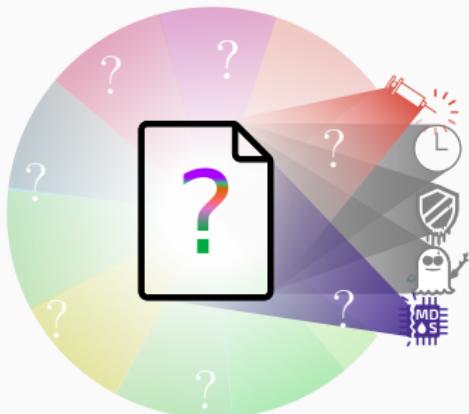
**Obs. 2.** Leakage detection overfits to known vulnerabilities.

We have mechanisms that **overfit** in

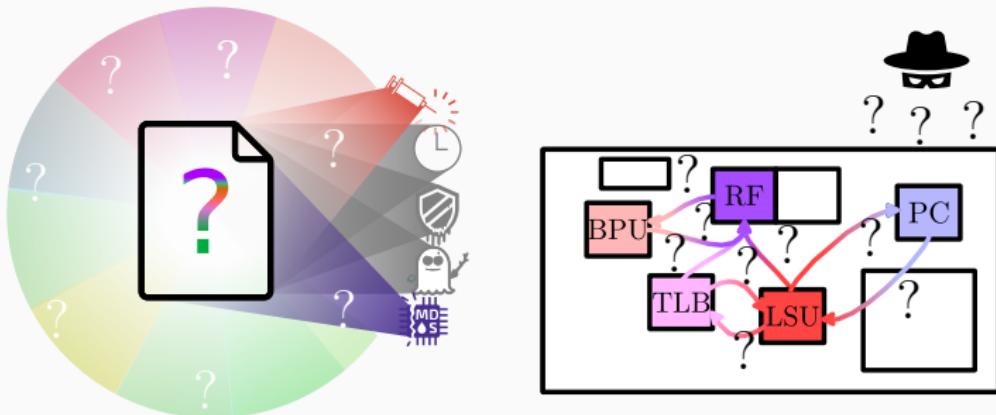
We have mechanisms that **overfit** in  
**Software**



We have mechanisms that **overfit** in  
**Software** and **Hardware**



We have mechanisms that **overfit** in  
**Software** and **Hardware**



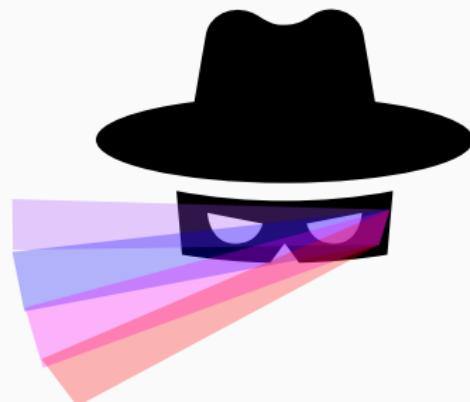
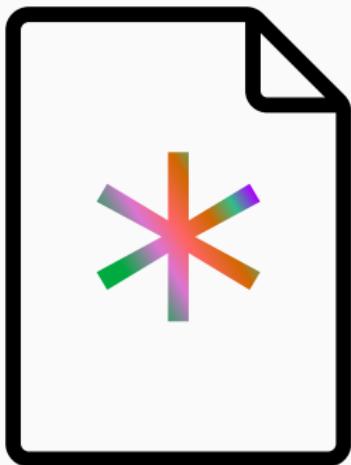
to known vulnerabilities.

We *need* mechanisms that **generalize** in

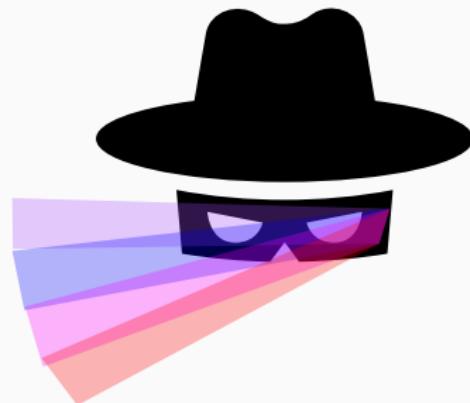
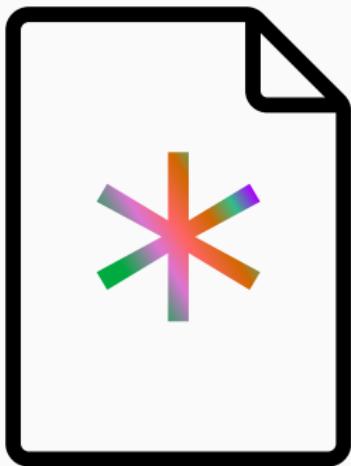
We *need* mechanisms that **generalize** in  
**Software**



We *need* mechanisms that **generalize** in  
**Software** and **Hardware**

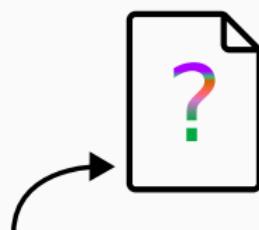


We *need* mechanisms that **generalize** in  
**Software** and **Hardware**



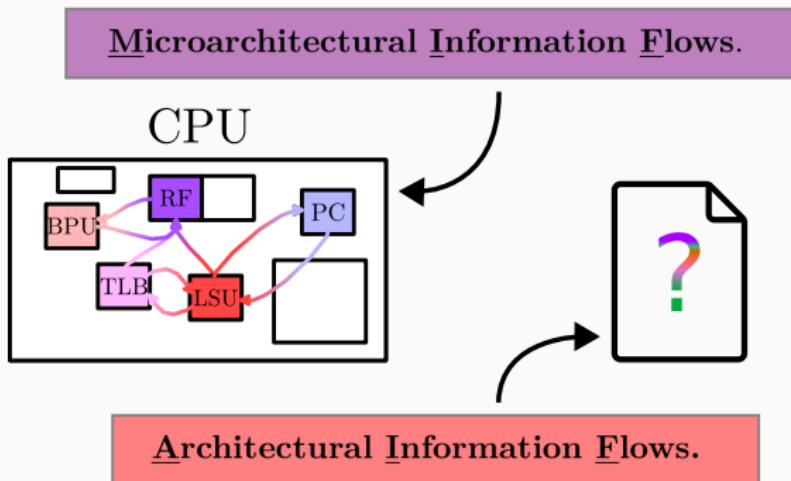
to **arbitrary vulnerabilities**.

# The Microarchitectural leakage Sanitizer

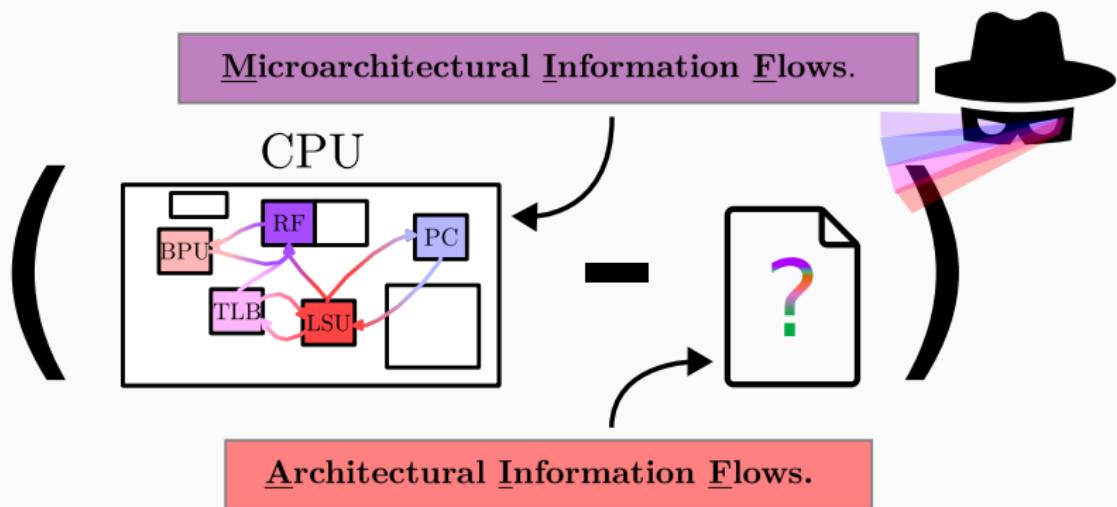


Architectural Information Flows.

# The Microarchitectural leakage Sanitizer



# The Microarchitectural leakage Sanitizer

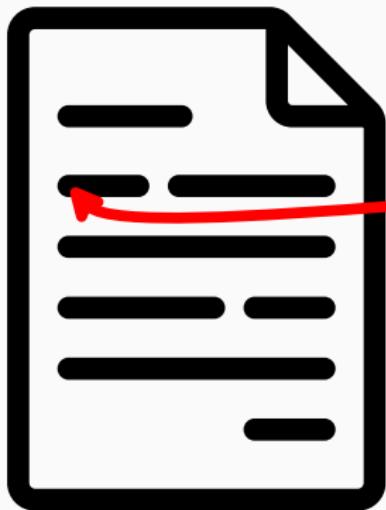


# The Microarchitectural leakage Sanitizer

**RQ. 1.** How can we compute the **architectural** information flows in hardware?

# Architectural info flows in software

SOFTWARE



MEMORY



# Architectural info flows in software

SOFTWARE



MEMORY



# Architectural info flows in software

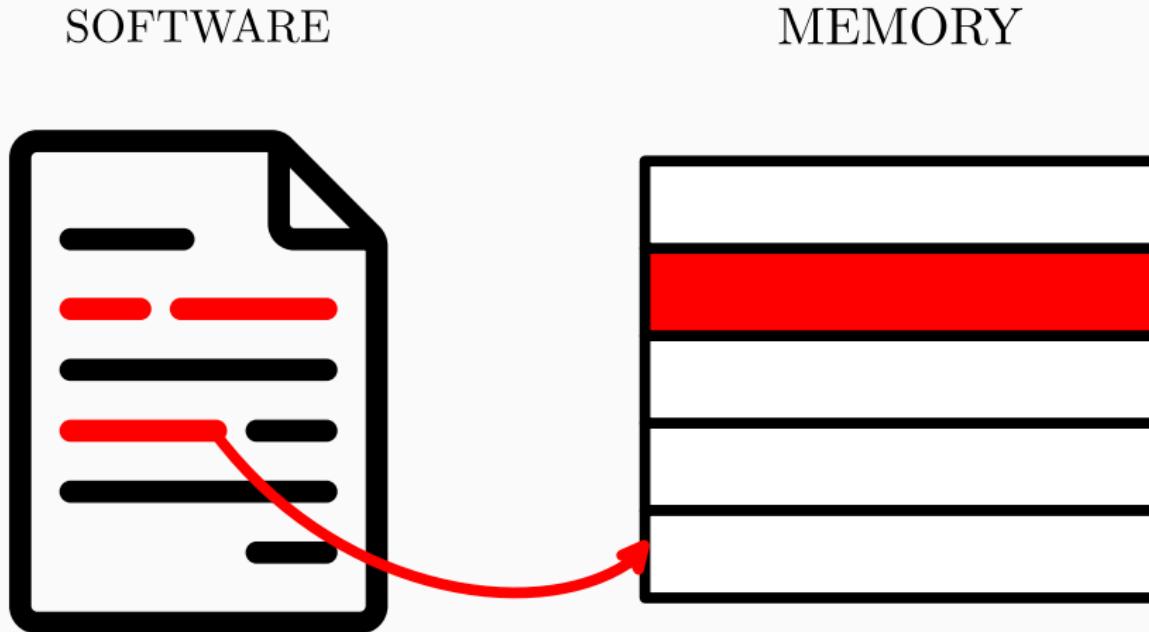
SOFTWARE



MEMORY



# Architectural info flows in software



# Architectural info flows in software

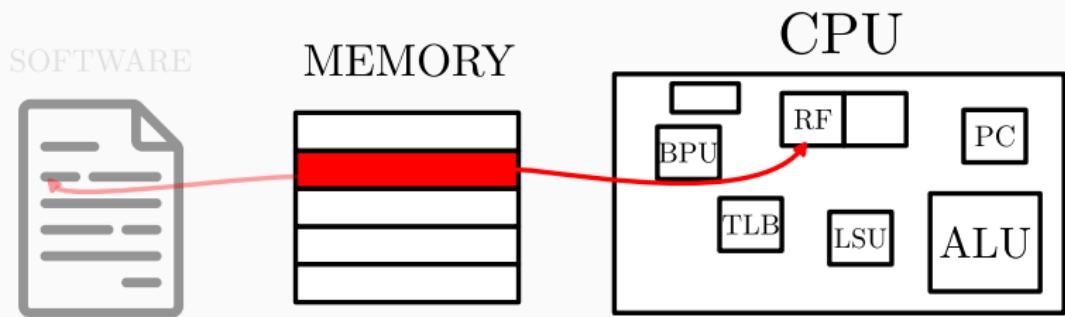
SOFTWARE



MEMORY



# Architectural information flows in *hardware*

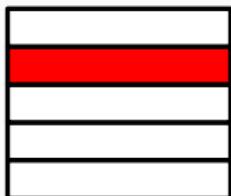


# Architectural information flows in *hardware*

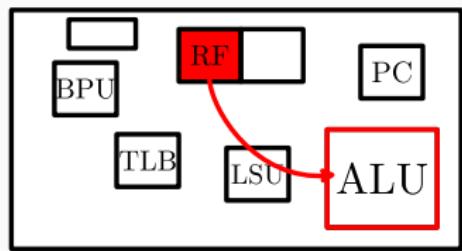
SOFTWARE



MEMORY



CPU

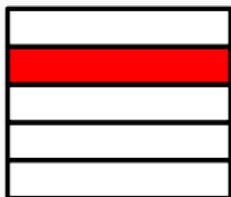


# Architectural information flows in *hardware*

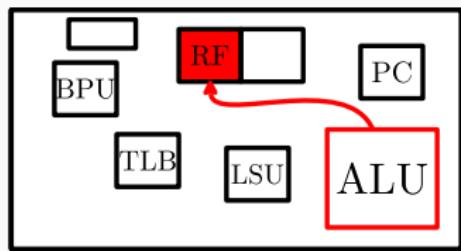
SOFTWARE



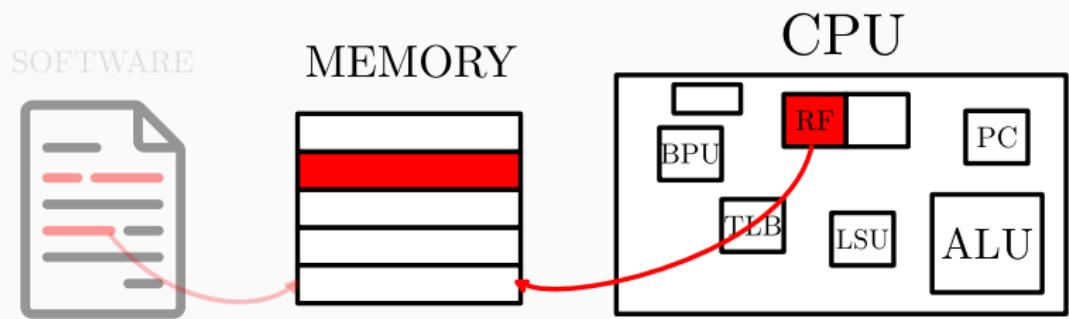
MEMORY



CPU



# Architectural information flows in *hardware*



# Architectural information flows in *hardware*

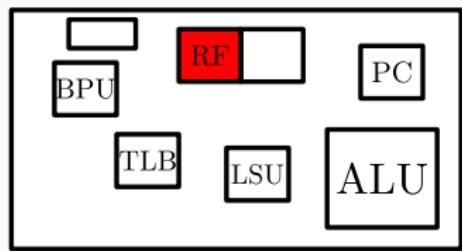
SOFTWARE



MEMORY



CPU



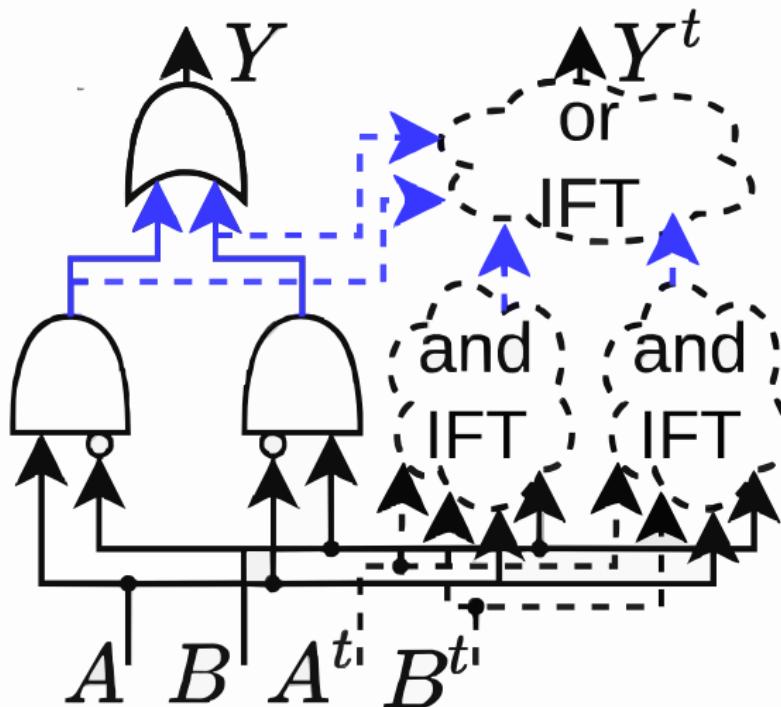
**Insight 1.** We can compute **architectural** information flows in *hardware* using *software* IFT.

# The Microarchitectural leakage Sanitizer

**RQ. 2.** How can we compute microarchitectural information flows in hardware?

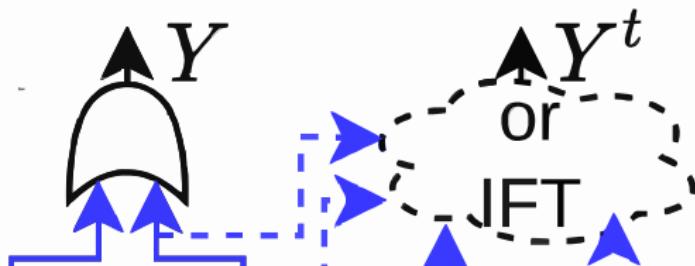
# The Microarchitectural leakage Sanitizer

CellIFT SEC'22

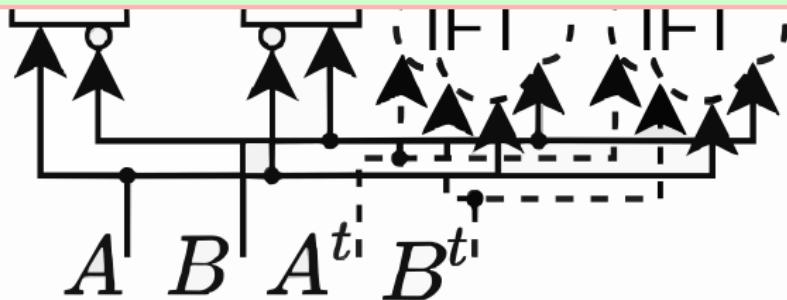


# The Microarchitectural leakage Sanitizer

CellIFT SEC'22



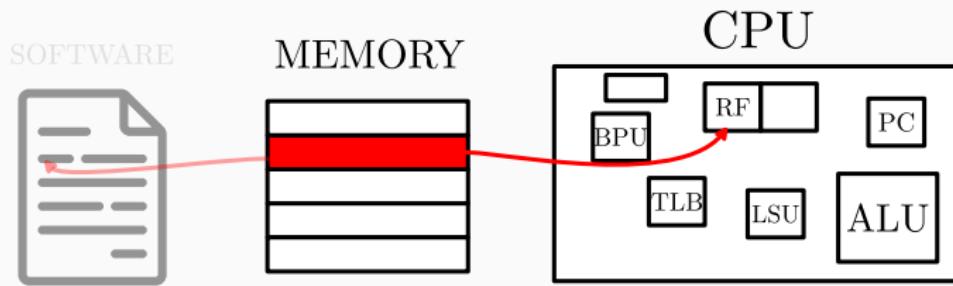
**Insight 2.** We can use existing methods for RTL taint tracking.



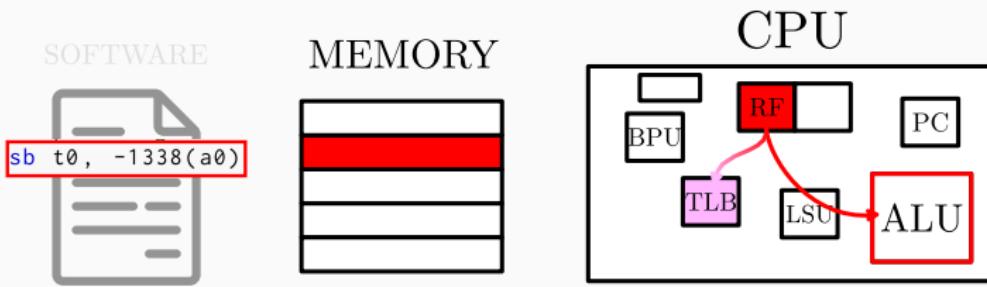
# The Microarchitectural leakage Sanitizer

**RQ. 3.** How can we detect leakage?

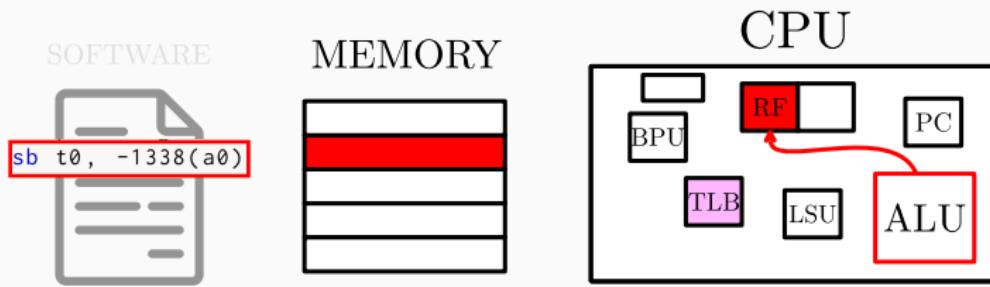
# Arch. and Microarch. Info Flows in hardware



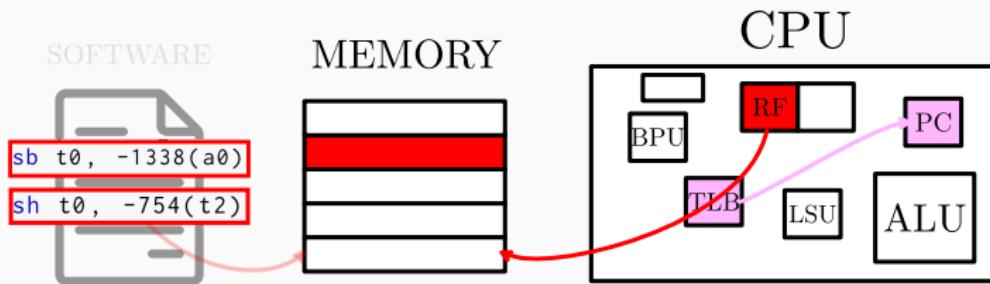
# Arch. and Microarch. Info Flows in hardware



# Arch. and Microarch. Info Flows in hardware



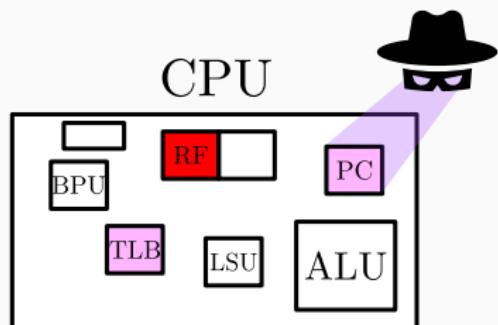
# Arch. and Microarch. Info Flows in hardware



# Arch. and Microarch. Info Flows in hardware

CVE-2025-29340 MEMORY

```
# Load some privileged data from S-mode.
0xa244c: lw $2, 450($ra)
...
# SPP=1, so we remain in S-mode.
0xa2ddd: sret
...
# The store executes transiently
# and leaks privileged data to the TLB.
0xa2ddc: sb $0, -1338($a0)
...
# SPP=0, so we go to U-mode.
0xd8f90: sret
...
# A store now leaks from the TLB.
0x67b50: sh $0, -754($t2)
```

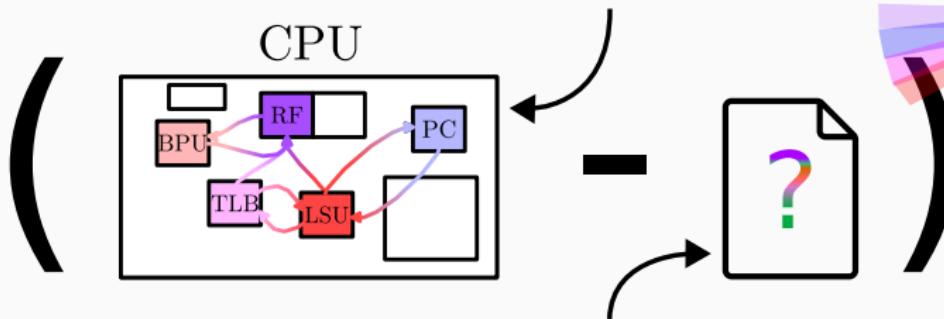


**Insight 3.** Exploitable leakage is a microarchitectural information flow to the PC!

# MileSan and RandOS

## Microarchitectural Information Flows

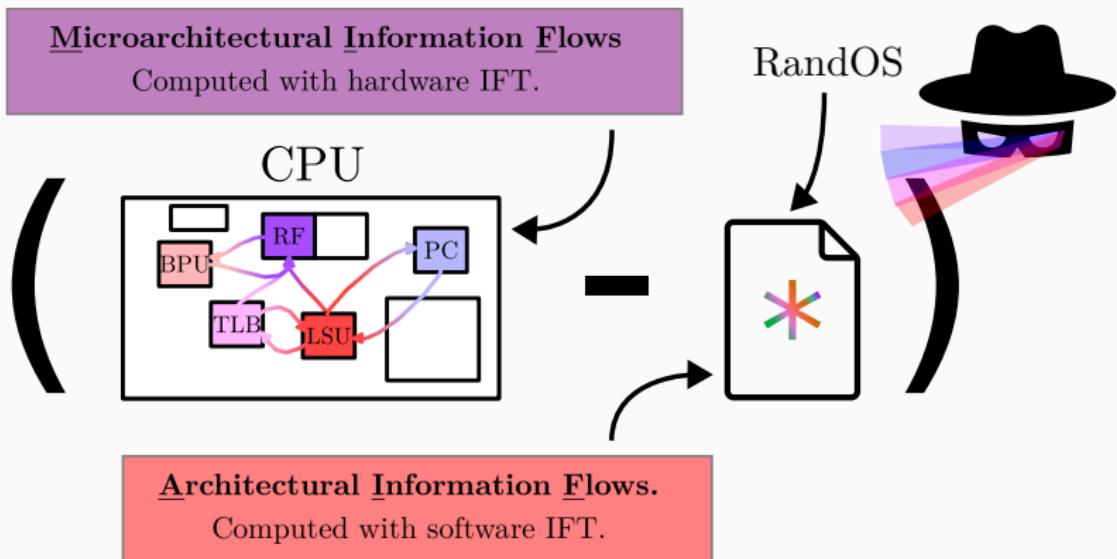
Computed with hardware IFT.



## Architectural Information Flows.

Computed with software IFT.

# MileSan and RandOS

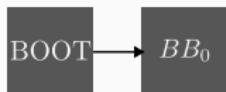


**RQ. 4.** How should test cases behave?

# RandOS: Generating programs

BOOT

# RandOS: Generating programs



# RandOS: Generating programs



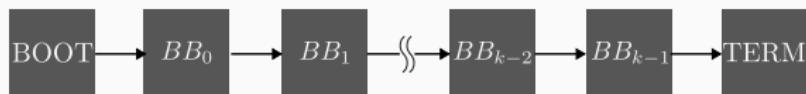
# RandOS: Generating programs



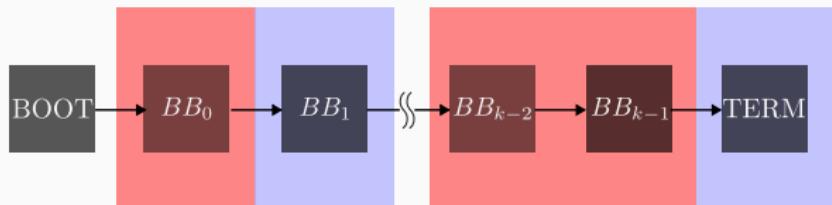
# RandOS: Generating programs



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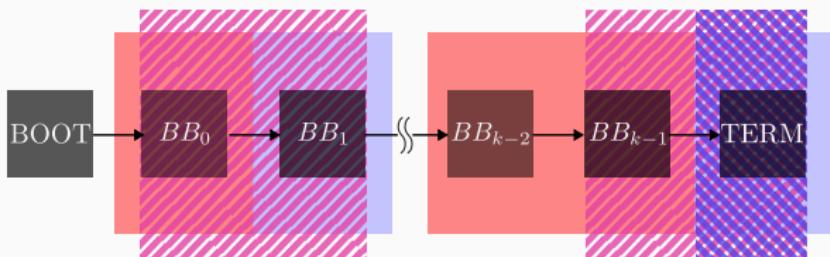


# RandOS: Generating programs



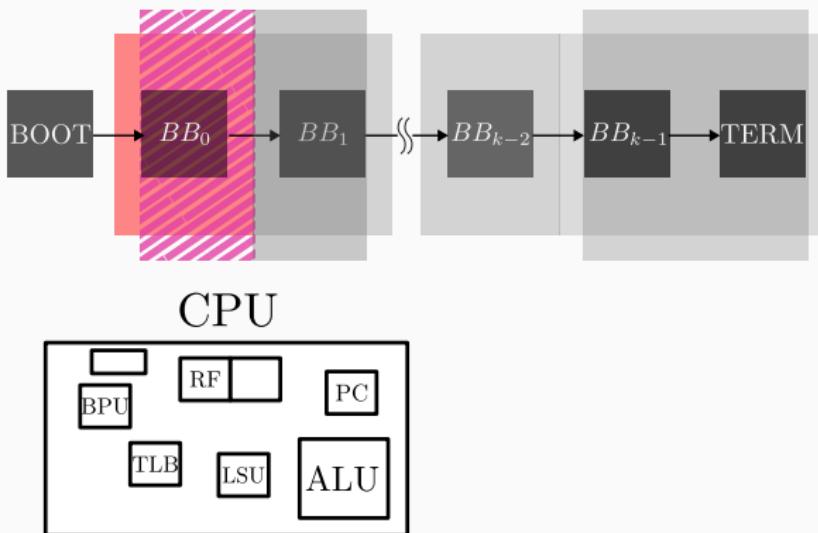
 privileges

# RandOS: Generating programs

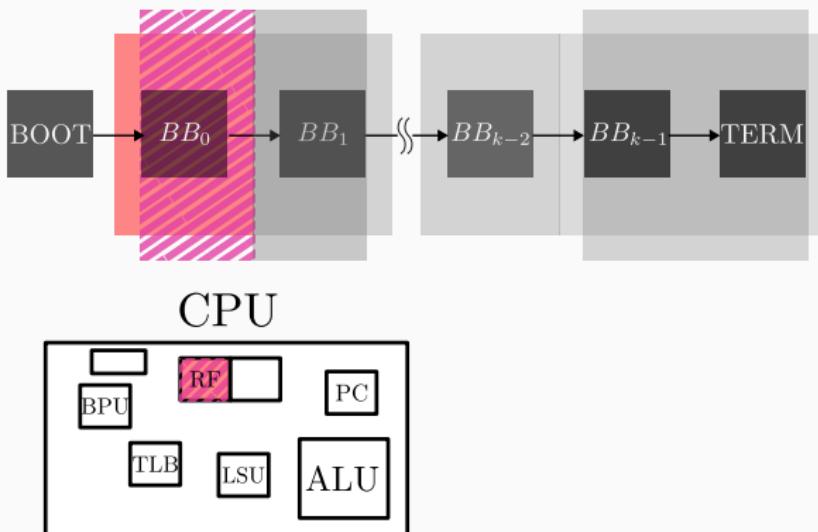


 privileges  
 address spaces

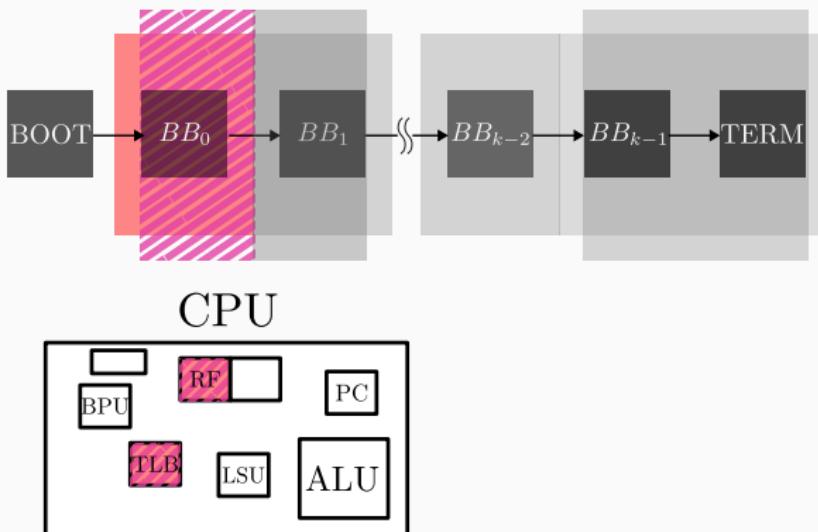
# RandOS: Traversing isolation boundaries



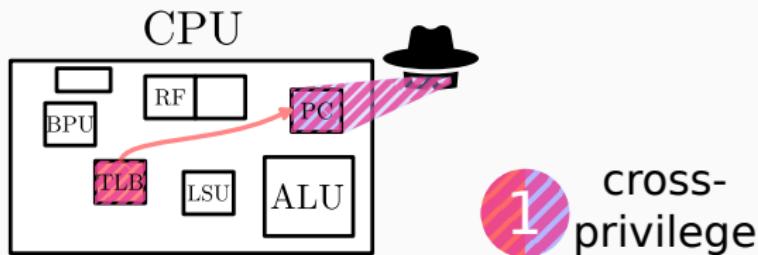
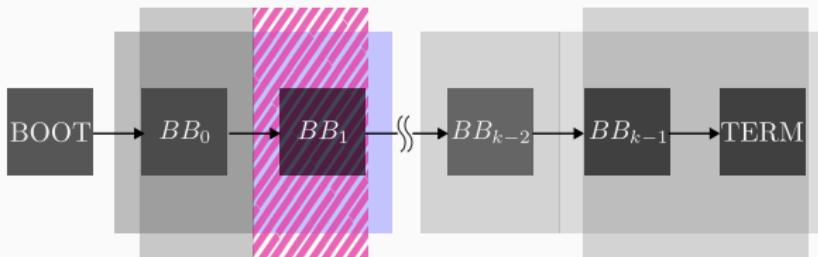
# RandOS: Traversing isolation boundaries



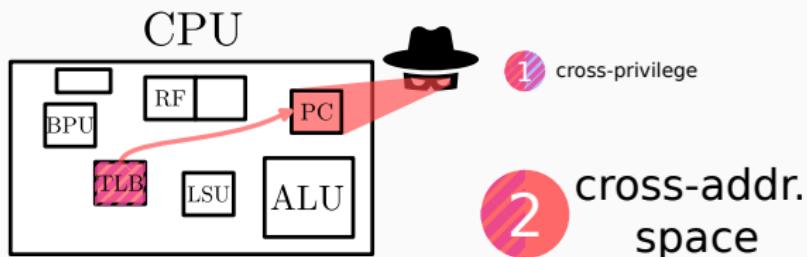
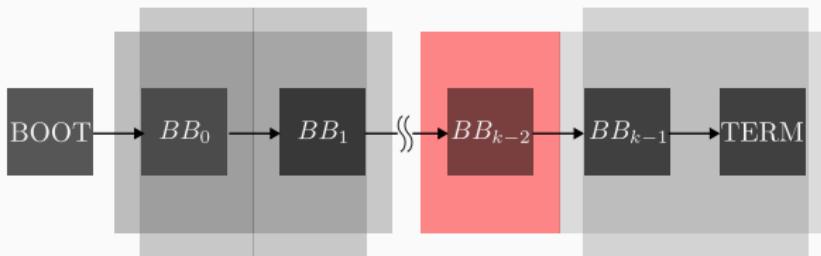
# RandOS: Traversing isolation boundaries



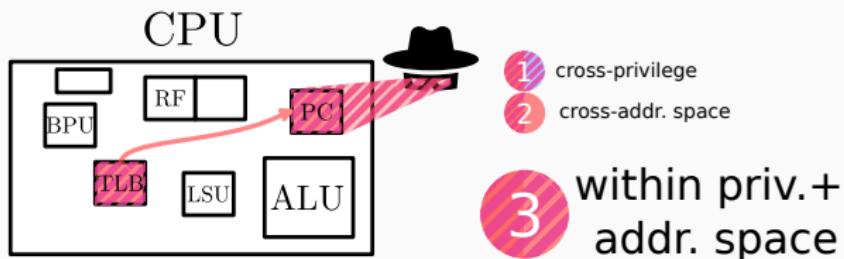
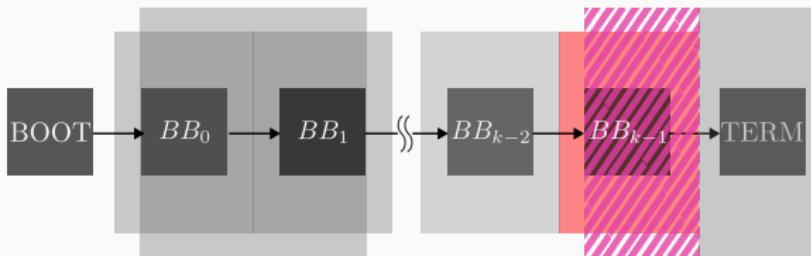
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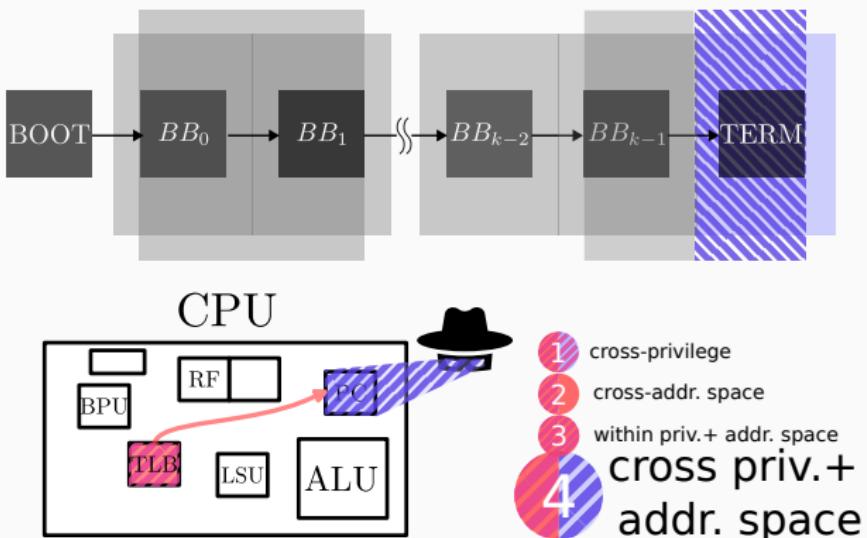
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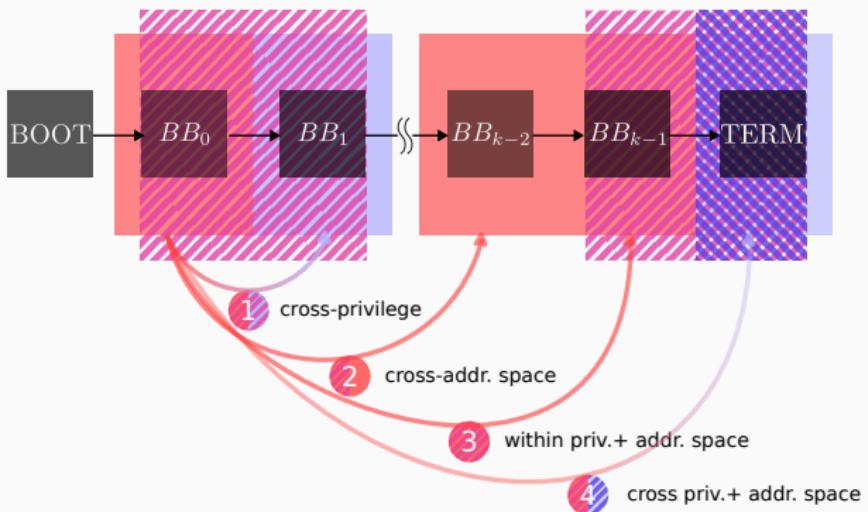
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# Implementation

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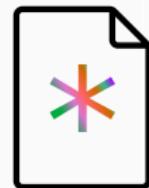


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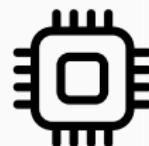
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**Q1.** How fast can MileSan and RandOS find known vulnerabilities? **4.5 $\times$  faster.**

**Q2.** Can MileSan verify PoCs from prior work?  
**Prior work reports false positives!**

**Q3.** Can MileSan and RandOS find new vulnerabilities?

# Can MileSan and Randos find new vulns.?

Vulnerability	DUT	Covert Channel
Spectre-V2-TLB	BOOM	TLB
Spectre-V4-TLB	BOOM	TLB
Spectre-RSB-TLB	BOOM	TLB
Trans. Meltdown	BOOM	TLB
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cp-Spectre-SLS	CVA6	TLB
MDS	CVA6	TLB
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Spectre-V1	OpenC910	DCACHE
Spectre-V1-TLB	OpenC910	TLB
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cross-  
privilege

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cross-  
privilege

# Can MileSan and Randos find new vulns.?

Leaking 1Mbps from kernel to user at 2GHz on BOOM

CVE-2025-29343

End-to-end exploit

```
...
0x28778: remu a2,s0,gp
0x28780: rem a2,a2,tp
0x287c8: divw ra,gp,a2
# Branch below mispredicted taken.
0x287d0: blt gp,ra,0x28e00
...
# Meltdown gadget executed transiently.
0x28e00: lb sp,-1587(ti)
0x28e04: lh s1,-1010(sp)
```

```
0 la ra, secret
1 la a2, buffer
... ...
# Evict the TLB, delay t0 results.
6 beqz t0, correct_target
7 ld a0, 0(ra) # Access secret.
8 andi a0, a0, 1 # Mask out a single bit.
9 slli a0, a0, 12 # Shift secret bit by page offset.
10 add a2, a2, a0 # Add secret bit to buffer.
11 ld a2, 0(a2) # Encode the secret bit in the TLB.
12 correct_target:
... ...
# Resume at correct path.
```

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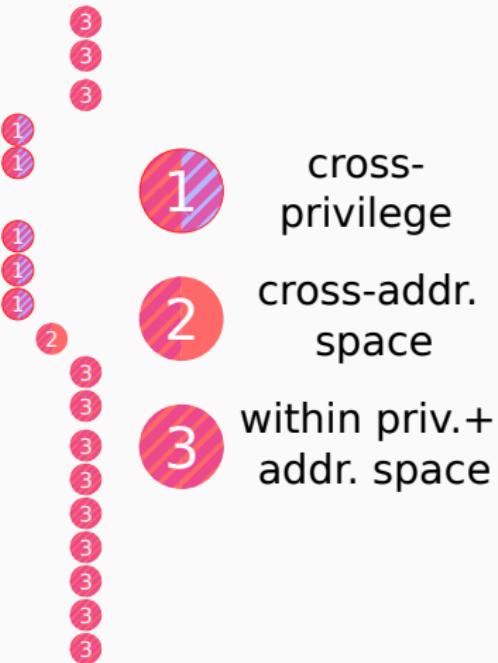
cross-privilege



cross-addr. space

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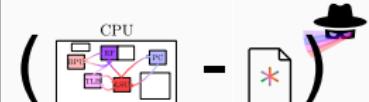
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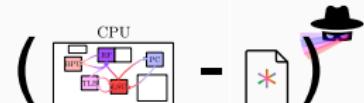
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more info + source code

