Trusted Silicon and Software design SoC / IP partner for Next Generation Wireless, AI & Power Management applications

SOPHIC (INTELLIGENT) SILICON TECHNOLOGIES

April 2025

SOPHIC (INTELLIGENT) SILICON TECHNOLOGIES

- Introduction
- Team
- Addressable Markets
- Analog IPs
- Digital IPs
- SoC / IP Development

INTRODUCTION

At Sophic Silicon Technologies, we empower Product and System Solution organizations with faster and best quality next generation Wireless, AI, Power Management and other Analog Mixed Signal + Digital **SoC** and IP Solutions. By leveraging deep RF/Analog mixed signal design and full chip SoC knowhow and rigorous design methodology, we deliver best-in-class-first SOCs/IPs.

Currently our team is working on development on next Generation Wireless Ips along with BT/BLE multi protocol SoC solutions.

Our organization is also source of various customized analog/mixed signal and digital IPs

TEAM

Sophic Silicon Team consist of engineers who has delivered the world best low power multiprotocol wireless chipsets along with different high speed SERDES designs.

Members has been WW project owner, architects and experienced RF, analog and digital designers for various products in large semiconductor organizations in past.

We strive for delivering best in class performance for BT/BLE WiFi7, Wifi6E, and Multiprotocol IPs and SoCs as part of Sophic Silicon

Our team also has great experience in High Speed Serdes design, Photonics IPs and different Analog/Mixed signal design's along with full SoC development

ADDRESSABLE MARKETS

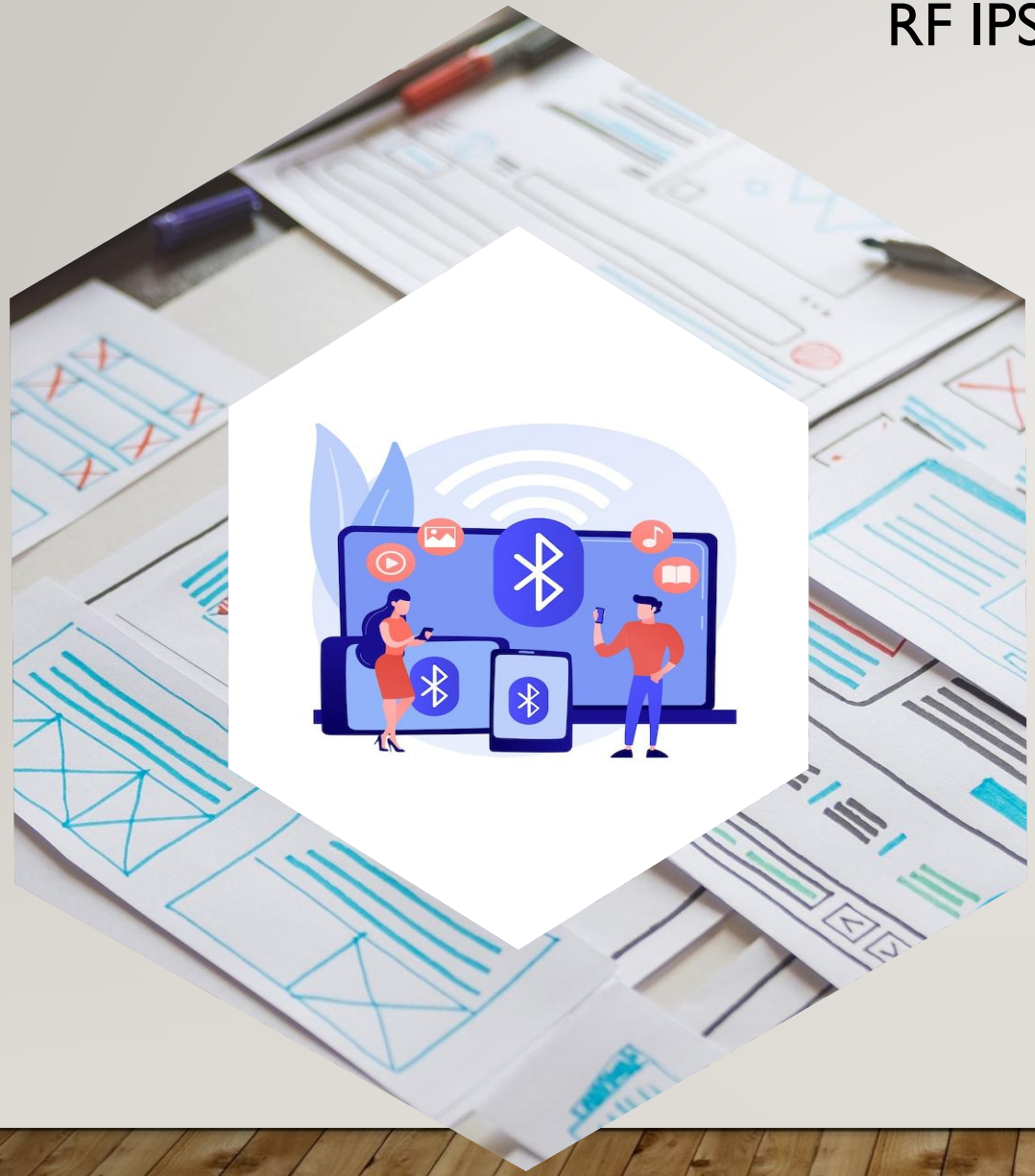
- Wireless SoCs and IPs
  - BT/BLE, 15.4 Dual band, ultra low power Multi-Protocol IPs and SoC
  - WiFi-6E & WiFi7 Analog/RF IP and SoC solutions
  - Wireless (Wi-Fi) Sensing and low power wake-up receiver unit
  - High performance & low power consumption IP Solutions
  - Low power BLE analog front-end design and BLE Audio
- AI Applications and Sensors
  - High Speed, Low Power ADCs and DACs
  - Blocks for cap, touch and other Sensors
  - Amplifiers and other IPs
- Power management solutions (Buck, LDOs, Full SoCs & Misc. circuits)
  - Low o/p load current very high efficiency I-PMU (good fit for wireless applications)
  - LDOs with different load currents
  - High Efficiency buck/ boost Regulator – low, Medium to high load current designs with less passive components
  - Energy harvesting Intelligent power management unit
  - Full SoC custom power Management solutions
- General Purpose Analog Mixed Signal & digital IPs

GENERAL PURPOSE MIXED SIGNAL IPS

- Reference Circuits
  - Bandgap, voltage and current reference circuits
  - General purpose Monitor ADCs
  - 12-bit SAR, low power
  - Sampling rate ADCS with 1-10 Mbps
- 14/12-bit DACs
- Crystal oscillator
  - Fast start-up and wide xtal frequency range support
  - Low Phase noise additions
- clocking circuits and Oscillators
  - General purpose and high frequency PLLs and DLLs
  - RC oscillator(s) with frequency tuning and self calibration
- Detectors
  - Supply Glitch Detector
  - ADC based Temperature Sensor
  - PVT Detector
- Specialized IO designs – based on customer request
- Specialized Analog Mixed signal IPs
  - SERDES Design- -> Our team has good knowhow & capability of 10Gbps to 56Gbps design and higher datarates
  - Sophic Silicon team has good knowledge of BiCMOS process and large (In GH) BW TIA or photonics IP development

Note -> All IPs has its own SPI or I2C interface for digital control

RF IPS & BLUETOOTH LOW ENERGY SIGNAL CHAIN



- Sophic Silicon has developed and are developing many RF IPs related to different protocol with state of art specifications. We have expertise in CMOS, GaN and BiCOMS processes.
- BT6.0 / BLE Signal chain Tx & Rx in FINFET process
  - Tx chain <2.8mA @0 dBm o/p power. 1.2V supply. O/P power range support -8 to 6 dBm in LP mode. Scalable to 20 dBm.
  - For Rx chain we are targeting ~2 mA or less current from 1.2 V supply. Sensitivity better than -100dB at chip port.
  - We support BLE Audio
  - Architecture supports extremely low, best in class connected idle power numbers numbers
  - We do support on-chip Intelligent power management (IMPU) design to support the full SoC
  - Signal chain design is complete and other SoC related features are in progress
- wake-up receiver (11ba)
  - State of art design
  - 1 Mbps, 2.5Ghz band, -98 dB or better sensitivity, with power consumption <~200uW

Note -> All IPs has its own SPI or I2C interface for digital control

POWER MANAGEMENT

- LDO (3.3V/1.8V)-> 0.6V-1.3V
  - 100uA-100mA load current, single cap, high PSRR design
  - 100uA-400mA load current, single cap, high PSRR design
  - All reference and start-up circuits included in blocks design
- Buck regulators
  - Low o/p current series
    - 1uA-1 mA >90% efficiency o/p tunable buck regulator
    - 10uA-100mA >95 % efficiency o/p tunable buck regulator
    - 1.8V/3.3V -> 0.6-> 1.25V o/p range
  - Mid to high o/p current series
    - 0.1mA-300mA > 95% efficiency o/p tunable buck regulator
    - 0.1mA-1000mA > 95 % efficiency o/p tunable buck regulator
    - 1.8V/3.3V -> 0.6> 1.25V o/p range
- Energy harvesting Smart PMU (S-PMU)
- Power Management SoCs with different ADC based and digitally controlled LDO/Buck/boost and LED drivers

Note -> All IPs has its own SPI or I2C interface for digital control

GENERAL PURPOSE DIGITAL IPS

- Various Digital IPs are available with all views and test benches
  - Interface IPs
    - I2C
    - I3C
    - SPI
    - QSPI
    - EUSART
    - I2S
    - SBC
    - JTAG
    - CAN
    - MIPI
    - RTC
  - PWM
  - PDM
  - ECC for Memories
  - Bus
    - AXI
    - APB
    - AHB
    - AHB Lite
  - JESD204C
  - LC3 Audio Codec
  - Processors
    - Customized RISC-V cores
    - Customized ARM cores subsystems

Note -> Please reach out for detailed datasheets etc. Also you can find more details on www.sophicsilicon.com

OUR SERVICES AND SOLUTIONS

THROUGH OUR SISTER ORGANIZATION

NEXTGENSILICON TECHNOLOGIES PVT LTD

WWW.NEXTGENSILICON.COM

System Engineering	Digital Front-End & Back-End	Analog Design & Layout	Embedded SW
Functional Requirement	RTL Design	Circuit design	Bootloader FW & BSP
System Modelling	Formal Verification	Analog / RF Layout	SoC FW/SW & SDK
Architecture and Design	Implementation & Physical Design	AMS Simulation and Automation	Device Drivers
FPGA Design & prototyping	DFT	Analog behavioural Modelling	Cloud Client & APIs
PCB Design & Simulations	Chip Bring-up & Lab Support	IP Modelling / AMS Verification	MCU SW

THANK YOU

www.SophicSilicon.com

www.nextgensilicon.com

Note - This document is Sophic Silicon Technologies Confidential. Must not be shared or distributed without permission of the organization.