VIETNAM NATIONAL UNIVERSITY HCMC

UNIVERSITY OF INFORMATION TECHNOLOGY

Presenter: Dr. Minh Son NGUYEN

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+84-8 3725 2002 Ext: 115, 152 | + 84-8 3725 2148 | www.uit.edu.vn | info@uit.edu.vn

VNUHCM Overview - Structure and Figures

Board of Regents

Strategic Division

CHANCELLOR AND VICE CHANCELLOR(S)

Science and Training Council

VNUHCM Office & 08 Functional Departments

Member Universities & Institute

27 Affiliated Units

LEARNER

90.000 Undergraduates

9.000 Graduates

HUMAN RESOURCE

6.500 Faculty & staff

TRAINING

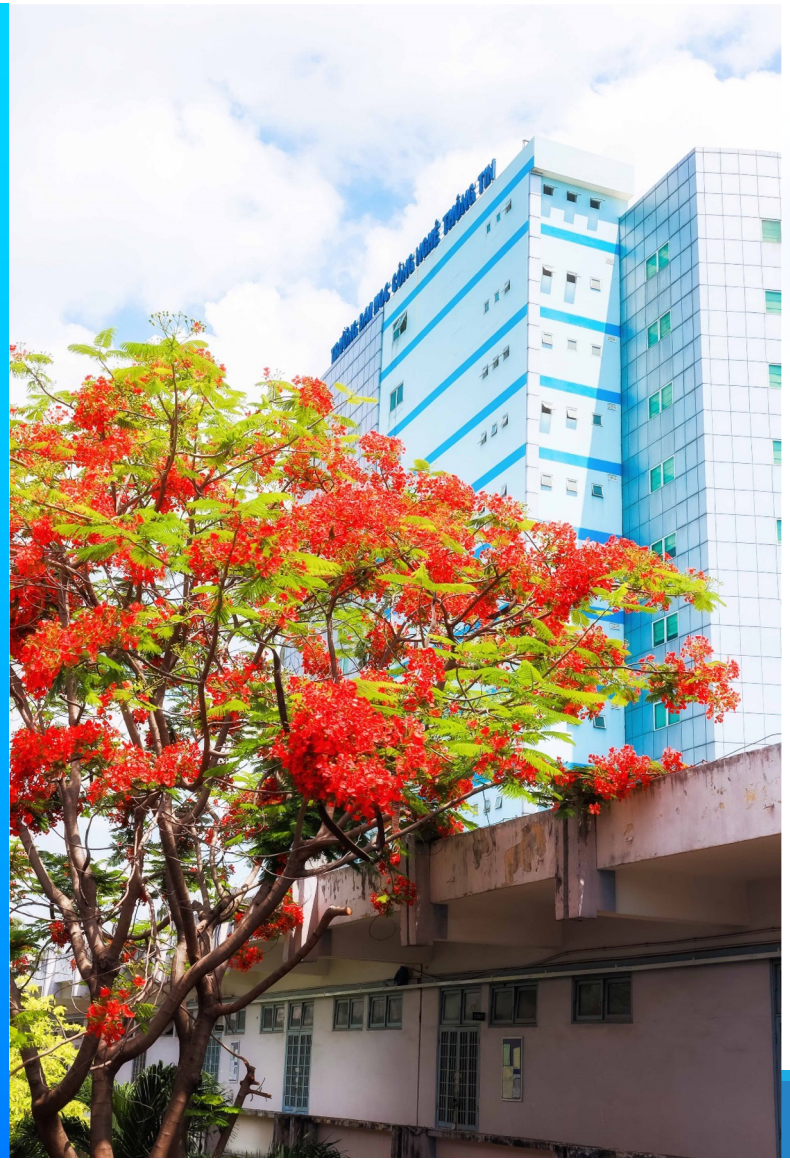
136 Bachelor programs
140 Master programs
90 Doctoral programs

RESEARCH

93 Laboratories
(13 Key laboratories)
#1 Inter. publication
in Vietnam (Scopus 2024)

VNUHCM - UIT

01
02
03
04



VNUHCM – University of Information Technology

Founding year: 2006

Field of Training:
Information and Communication Technology

A member of prestigious VNU-HCM

Vision

Become a prestigious university in Information and Communications Technology (ICT) and other related fields in the Asian region.

Number of

Employees

Update until Oct 2025

95

Professors/Ph.D Lecturers

152

M.Sc. Lecturers

Lecturers are alumni from prestigious universities in developed countries such as the UK, France, the United States and Japan, etc.

List of Lecturers

VNUHCM - UIT

05
06
07
08

Number of

Students

Update until Oct 2025

Student enrollment score

Major	2022	2023	2024
E-Comerce	27,05	25,8	26,12
Data Science	26,65	27,05	27,5
Computer Science	27,1	26,9	27,3
Computer Net. and Com.	26,3	25,4	25,7
Software Engineering	28,05	26,9	26,85
Information System	26,7	26,2	26,25
Computer Engineering	26,55	25,6	26,25
Artificial Intelligent	28	27,8	28,3
Information Technology	27,9	26,9	27,1
Information Security	26,95	26,3	26,77
IC Design			26,5

10.868

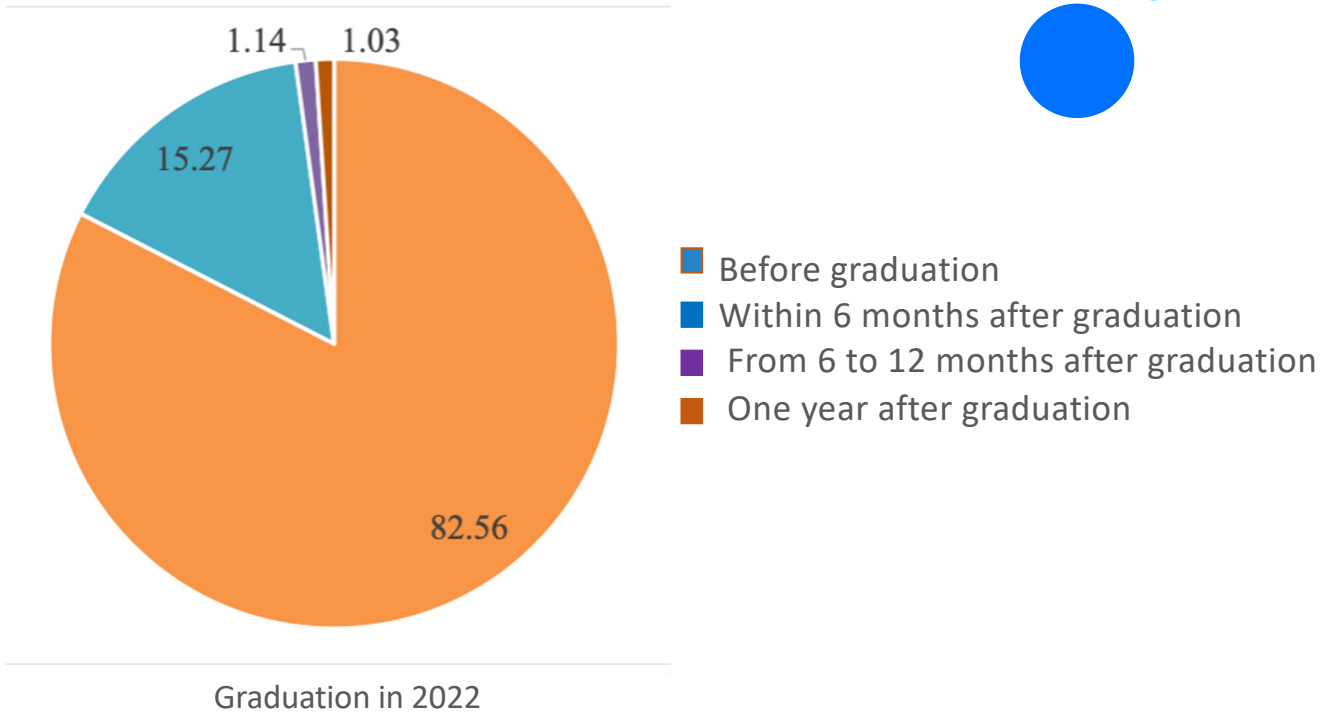
Enthusiastic Undergraduate

550

Professional Graduate

Specialized & Exclusively in IT and Computer Science majors.

Student Employment Rate



COMPUTER ENGINEERING

INTRODUCTION TO FCE

DR. MINH SƠN NGUYEN

FACULTY DEAN OF COMPUTER ENGINEERING

HEAD of ASICLAB

UIT, Dec 16 2025

TS. Nguyễn Minh Sơn

Trưởng Khoa

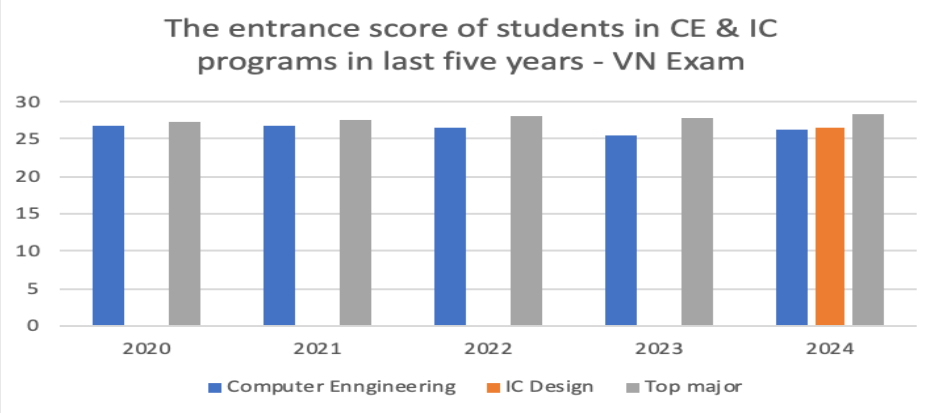
Tốt nghiệp ngành Kỹ thuật Máy tính, Trường Đại học Bách Khoa, ĐHQG-HCM. Ông được cấp bằng Tiến sĩ ngành Electrical Engineering tại Đại học Ulsa, Hàn Quốc.

Email: sonnm@uit.edu.vn

NUMBER OF STUDENTS 2025

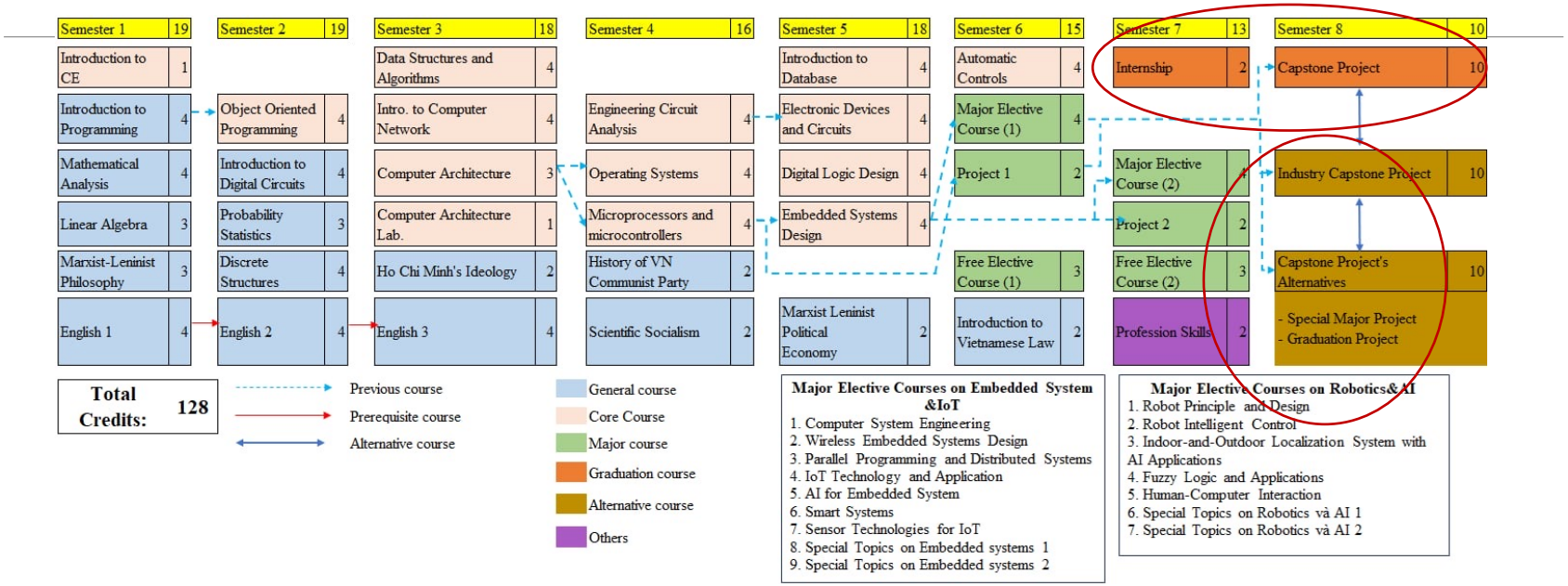
COMPUTER ENGINEERING

FCE students				
2024			2025	
Grad.	14		0	
Under.	1034		1268	
Stud./Yr.	317	8.7/10	**325**	**8.5/10**
Bach.CE	226	26.2	225	25.3
Bach.IC	91	26.5	**100**	27.0
Ms.CE	14		**22**	



CE CURRICULUM 2024

COMPUTER ENGINEERING



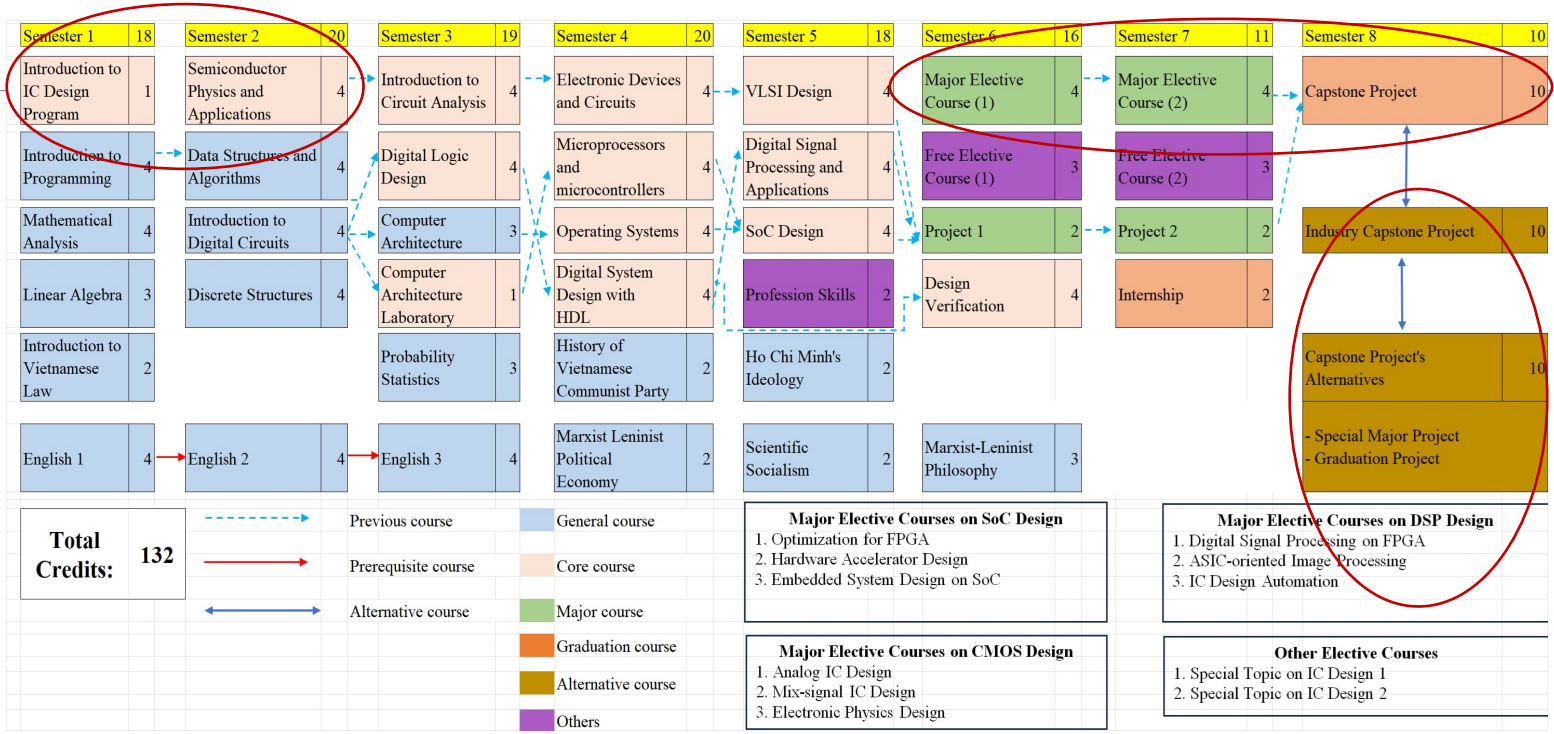
8 semesters

Major in IoT

Major in **Robotics and AI**

IC DESIGN CURRICULUM 2024

COMPUTER ENGINEERING



IC DESIGN ENGINEERING

8 semesters

132 credits

- CMOS IC Design
- System-on-Chip Design
- DSP Design

MASTER PROGRAM 2024

COMPUTER ENGINEERING

UNDERGRAD PROGRAM	MASTER OF COMPUTER ENGINEERING													
4 YEARS	YEAR 1								YEAR 2					
1- Bachelor of Computer Engineering 2- Bachelor of IC Design 3- Bachelor of EE & Automation Control 4-Bachelor of CS/IS/SE/IT/DS	Track 1	Research Based Method 1	Semester 1	7	Semester 2-4							53	Total Credit	
			Phylosophy	3	Research-Based Thesis –Method 1							53	60	
			Scientific Research Methodology	2										
			Advanced Scienctific Research Methodology	2										
	Track 2	Research Based Method 2	Semester 1	14	Semester 2	20	Semester 3	12	Semester 4		15			
			Phylosophy	3	Advanced VLSI Design	4	Major Elective course	4	Research-Based Thesis – Method 2		15	61		
			Scientific Research Methodology	2	Advanced ASIC Design	4	Research Project on Embedded System & IoT	4						
			Mathematics in Computer Engineering	3	Advanced Embedded Systems Technologies	4	Research Project on IC Design	4						
			Advanced Computer Systems Engineering	3	Advanced IoT Technologies	4	Preparation for Thesis							
			Management and Leadership Skills for Computer Engineering	3	Research Topic	4								
	Track 3	Application-Based	Semester 1	14	Semester 2	20	Semester 3	16	Semester 4		12			
			Phylosophy	3	Advanced VLSI Design	4	Major Elective course 1	4	Application-Based Thesis		12	62		
			Scientific Research Methodology	2	Advanced ASIC Design	4	Major Elective course 2	4						
			Mathematics in Computer Engineering	3	Advanced Embedded Systems Technologies	4	Major Elective course 3	4						
			Advanced Computer Systems Engineering	3	Advanced Internet of Things Technologies	4	Major Elective course 4	4						
			Management and Leadership Skills for Computer Engineering	3	Research Topic	4								

Major Elective Courses in IC Design

1. Semiconductor Manufacture Process Technologies - 4
2. IC Packaging Technologies - 4
3. SoC Design Technology for AIoT - 4
4. Advanced Mixed-Signal Integrated Circuit Design - 4

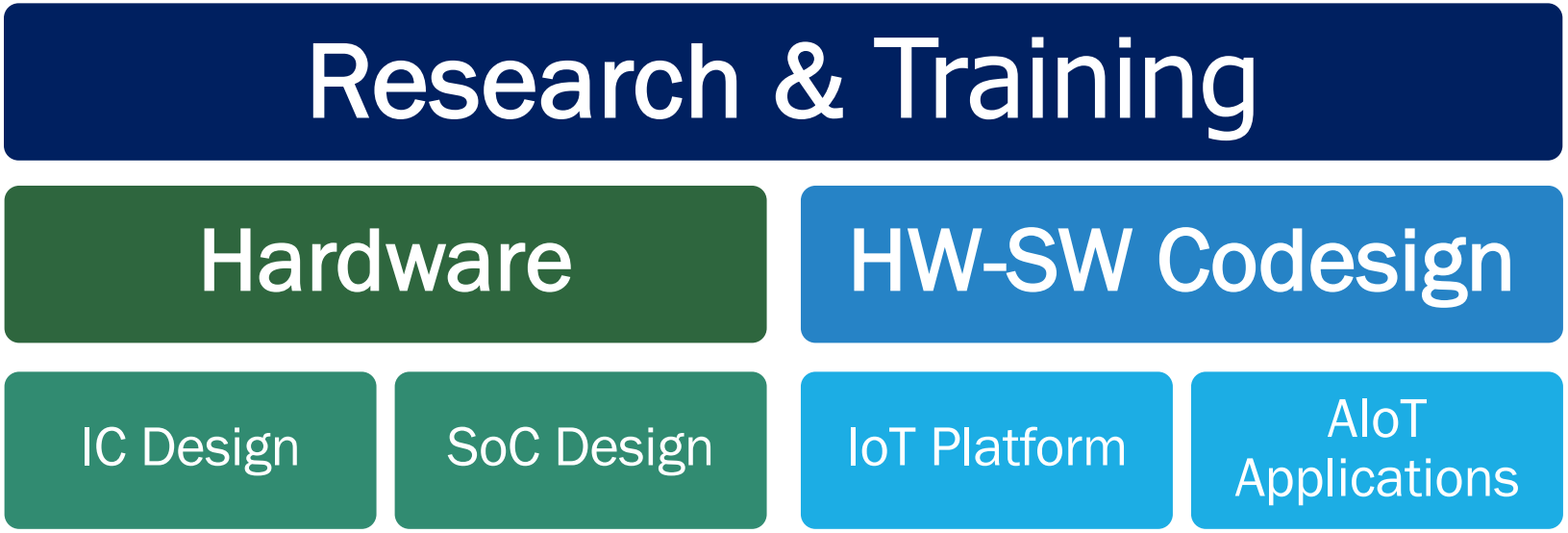
Major Elective Courses in AI&IoT

1. Cloud and Edge Computing - 4
2. Application of Artificial Generative Intelligence - 4
3. Parallel System Programming with GPU - 4
4. Edge AI Technologies - 4
5. Special topic 2 [Industry-orientedTechnology Topic] - 4

COMPUTER ENGINEERING

Introduction to ASICLAB

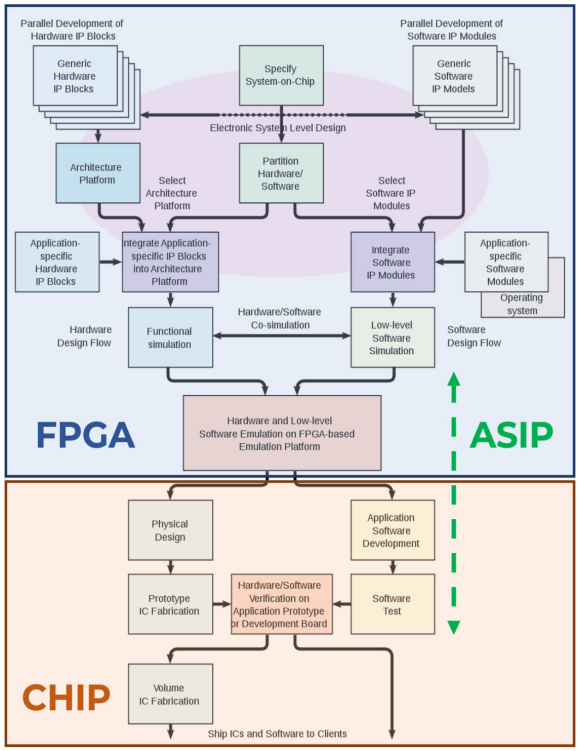
Focuses on the principles and methodologies involved in the design and development of IC & System on Chip Design, AIoT and Its applications.



COMPUTER ENGINEERING

ASICLAB - Facilities

LAB Methodology



LAB Equipment

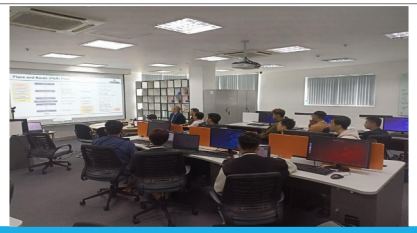
SW tools	EDA – Cadence (Virtussoo, Inovus,…) FPGA – Xilinx (Vitis AI, Vitis HLS)
Server	A4USA003 (16 Cores, 196 GB RAM, 4 TB SSD) ALVEO 250
DEV. KIT	Vertex- 7 FPGA VC707 Zynq 7000 SoC KRIA KV260 VISION AI
Measurement tools	Tektronix TDS2012C Tektronix Mixed Signal Oscilloscope MSO54 Keysight 16862A 68-Channel Portable Logic Analyzer N5172B EXG X-Series RF Analog Signal Generator, 9 kHz to 6 GHz

COMPUTER ENGINEERING

ASICLAB – Research and Training

Dr. Nguyen Minh Son

Director



PI & Co-PI

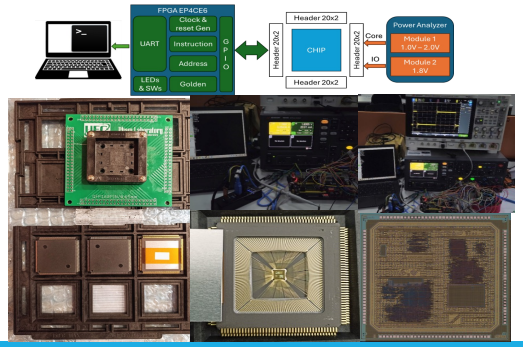
RTL R&D Team

DV R&D Team

PD R&D Team

ES R&D Team

Prototypes



Short Course training

1- Logic Design & Synthesis
2- Design Verification
3- Physical Design

Lab tools:
Cadence – Innovus, Xcelium, Genus, Virtuoso
SoC KIT – ZC 05, ZCU 102, ZCU 129

COMPUTER ENGINEERING

ASICLAB – Research and Training

09
Research Assistants

17
Research Interns

16
Collaborating Lecturers

Director

Dr. Nguyen Minh Son

Key Members

MSc. DucTT

MSc. TungTT

BE. ThinhTQ

BE. PhatNT

Research Advissors

Prof. Tanaka Kiyofumi

Prof. Pham Cong Kha

Prof. Dirk Slama

Bach Luong

Phil Hoang

Van Le

Training Activities – Design Verification Course

- Course Objective: the participants will be able to build a basic testbench to verify an RTL design using a modern method in Universal Verification Methodology.
- Course Format
  - ✓ The course consists of nineteen sessions.
  - ✓ The first seven sessions cover basic understanding of building a UVM testbench in three phases. We will study how to build the testbench components in each phase. In
  - ✓ The remaining twelve sessions, apply the knowledge to verify a SPI controller, follow the industry standard procedure that includes verification planning, testbench construction and coverage closure.
  - ✓ The teams will present their work according to the given format.
- Tools: The source code in the labs and lab_solutions was designed to run on both Cadence Xcelium tool as well as Siemens Questa tool. The Makefiles list the command syntaxes used to invoke Xcelium or Questa.

Training Activities – Design Verification Course

Section	Tasks	Duration
SystemVerilog and Fundamental Verification Concepts	**Introduction**: course objectives and prerequisites **Lecture:** 1) SystemVerilog - Interface - Aggregate data type - Package - Class - Randomization and constraint block - Covergroup and coverpoint **Lab:** - exercise1.sv - exercise2.sv - exercise3.sv - inf_lab.sv **Lecture:** 2) What is verification? 3) Basic understanding of verification planning - Generation of verification requirements derived from the design specification - Three-phase testbench construction + Phase 1: Stimulus generation + Phase 2: Data checking + Phase 3: Capture of functional coverage - Verification closure using functional coverage metrics	Days 1,2,3 6 hours

Section	Tasks	Duration
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Training Activities – Design Verification Course

SPI TB P1 Planning Class Project	**Lecture**: Review of the SPI specification. Discussion on the format of a verification plan. **Lab:** Create an Excel file that lists all verification requirements. **Lecture:** Discussion on how to create a SPI interface and an APB interface. **Lab:** Create spi_if.sv, apb_if.sv and clk_rst_if.sv to be saved in the resource database. **Lecture:** Discussion on how to create the TLM transaction. **Lab:** Create a spi_tlm package named spi_tlm_pkg.svh that contains the class definition of spi_tlm class. **Lecture:** Discussion on how to create a Makefile to compile the testbench in steps.	Days 10,11 4 hours

CERTIFICATE OF COMPLETION

PRESENTED TO

Trần Nguyên Giáp - 22520365

for completing the

ADVANCE DESIGN VERIFICATION

a course conducted by Tresemi organization
from February 15, 2025 to May 19, 2025,
in partnership with the University of Information Technology – VNUHCM.

VAN LE
Instructor, Tresemi

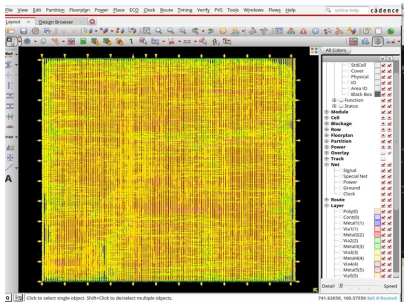
DAVID CAMPBELL
Executive Director, Tresemi

MINH-SON NGUYEN
Dean, Faculty of Computer Engineering, UIT

TRESEMI
EMPOWERING TOMORROW'S LEADERS

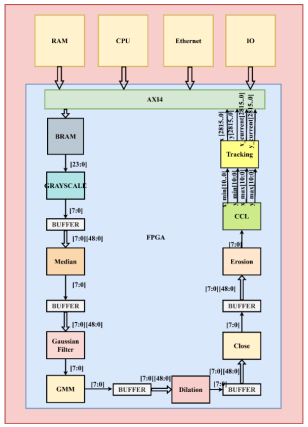
Research Activities

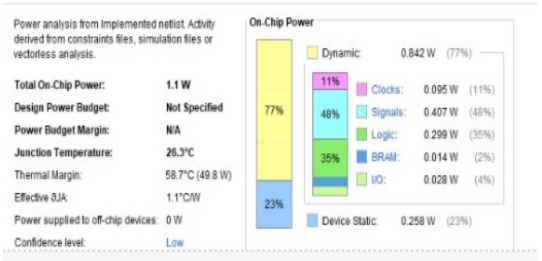
Year	Research Project			Students Projects
	HCMG	VNUHCM	UIT	
2020	2	3	4	26
2021	1	1	5	34
2022	2	1	12	20
2023		5	5	40
2024		7	12	58
2025	1	4	6	28



	RISC-V Steel MCU (This work)	RISC-V MCU [3] (2020)	RISC-V SoC [11] (2022)
Core	Steel Core	VexRISCV	VexRISCV
Process	CMOS 45 nm	SOTB 65 nm	CMOS 65 nm
Frequency (MHz)	100	156	50
Area (μm²)	644,680	1,323,640	15,963,580
Core Vdd (V)	0.9	0.6	N/A
Power (mW)	13.52	5.21	42.1

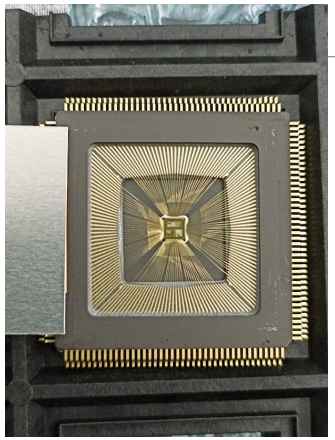
uC RISC 32 bits

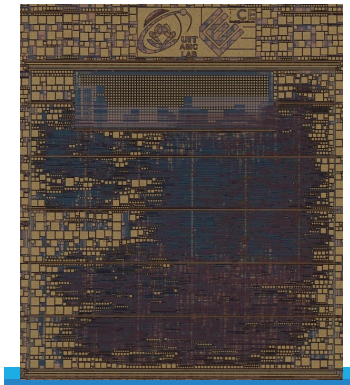




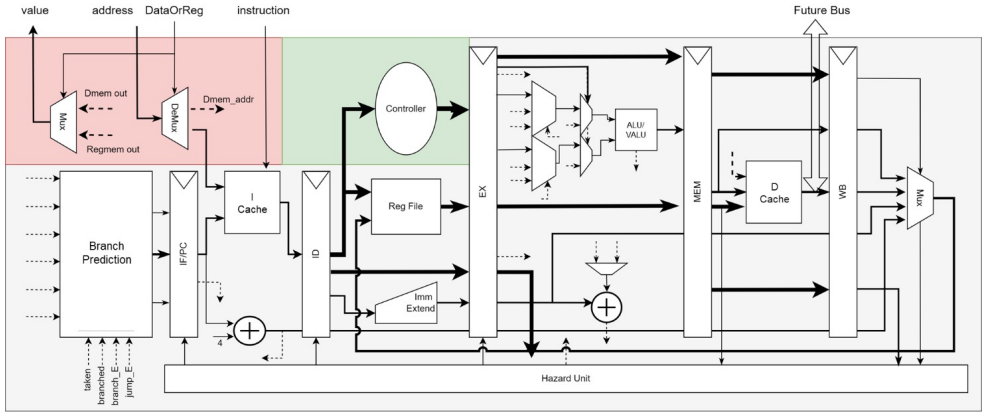
AI Accelerator for Image procesing

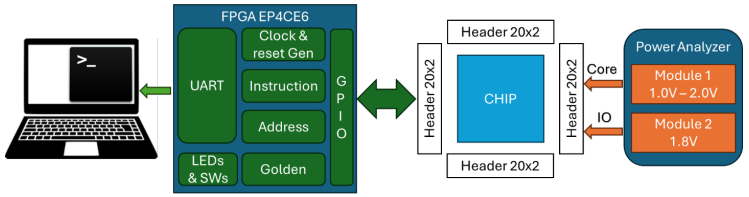
Research Activities – Publications





RISC-V 32 bits uP using 180nm ROHM





Physical Stats

Area: 918.96 × 917.28 µm

Core Size: 898.8 × 897.12 µm

No. Pins: 32 Pins

Cache: 512 Bytes

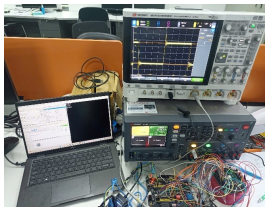
Performance

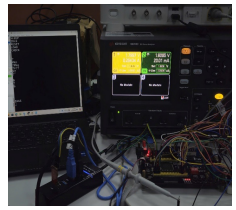
Designed Freq: 50 MHz

Fmax: 60 MHz

Power consumption: 61.63 mW

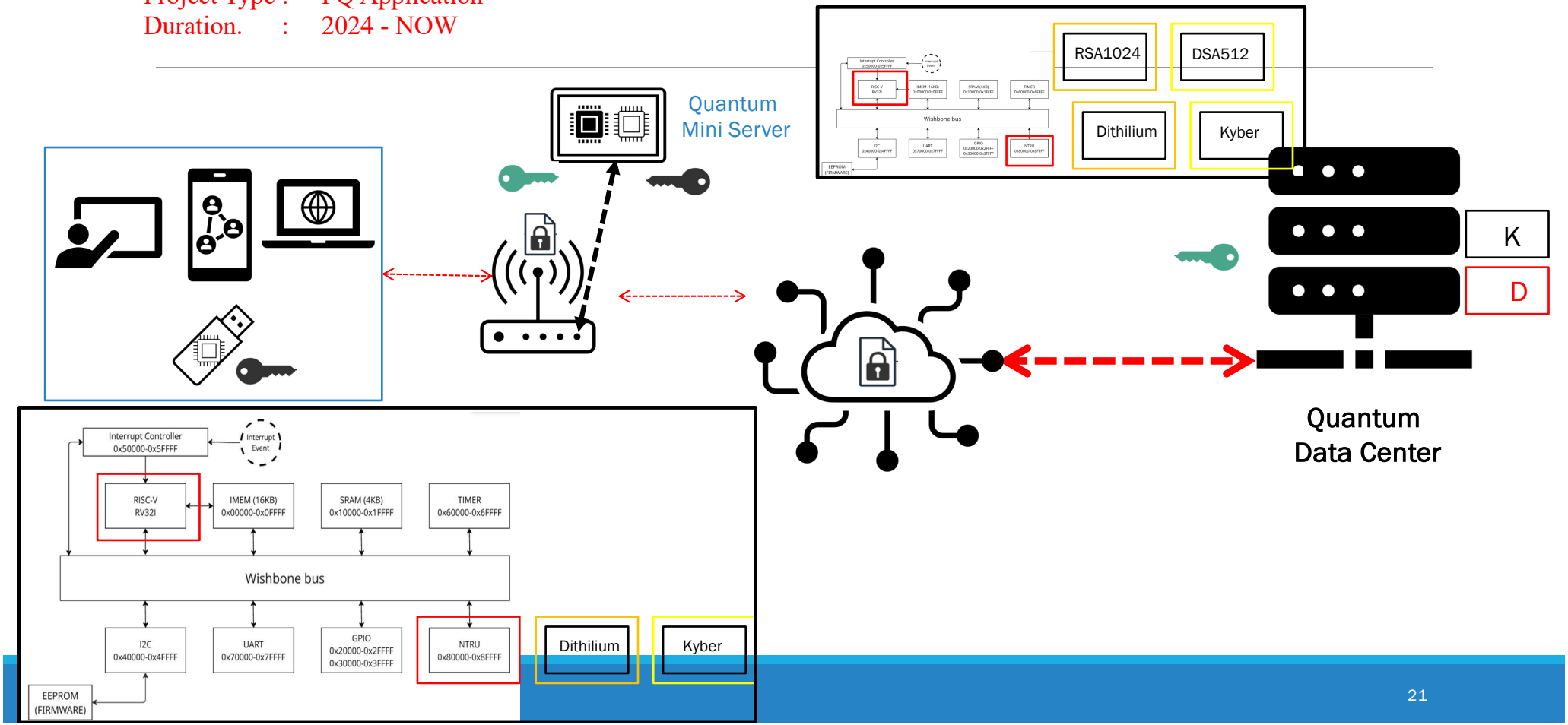
Voltage: 1.8 V





R&D Projects – Payment/Passkey for PQC applications

Funded by.
Project Type : PQ Application
Duration. : 2024 - NOW



ASIC LAB PARTNERS

Thank you!