SILTEST Semiconductors

POST-SILICON SERVICES

Packaging/Test/Qualification/Production

April 2025

info@siltest.com
www.siltest.com

Vision

Shaping the Future of Semiconductor Testing as a Leading Engineering Services Partner

Mission

To empower our clients in the semiconductor industry to bring their products to market faster, more efficiently, and with the highest quality.

Our Values

COMPANY PROFILE

Founded in **2023**
Team of back-end experts, HQ in **Germany**

01
KEY FIGURES

Digital, Neuromorphic , High-speed, Analog, Mixed-signal, RF

02
PRODUCT TYPES

AI, Data Centers, Consumer, Industrial, Automotive, Military

03
MARKET SEGMENTS

Teradyne, Advantest, NI, LTX, Microtest, Chroma, Custom solutions

04
ATE KNOWLEDGE

DRIVING TIME-TO-MARKET AND PROFITABILITY FOR OUR CUSTOMERS

OUR SERVICES PORTFOLIO – FROM ENGINEERING, TO INFRASTRUCTURE, TO TALENT DEVELOPMENT

Engineering Services

A collaborative and innovation driven approach to **Chip design, testing**, **qualification** and **product engineering** services

Tools and Automation

AI-powered, integrated tools to accelerate product development, enhance **productivity**, **quality** and **cost**

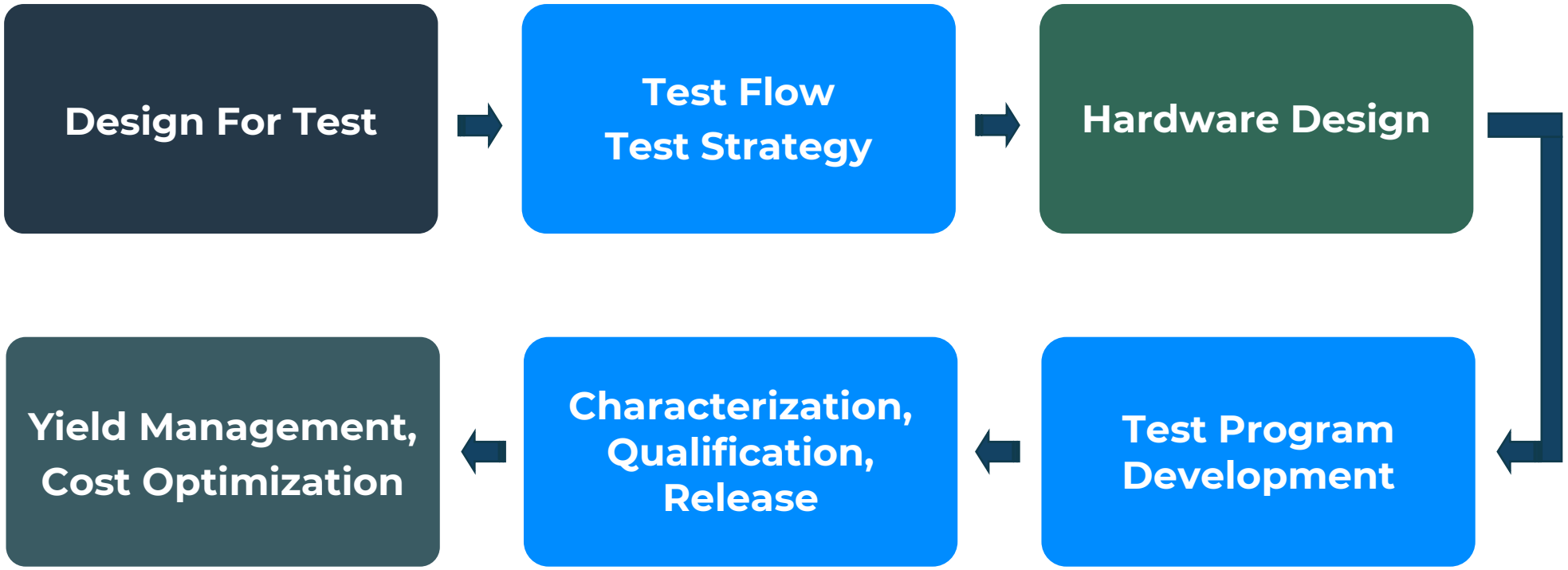
Infrastructure Services

Access to an advanced **packaging & test** facility for all your post-silicon testing needs, fully located **in European Union**

SilTest Academy

Nurture and Train next generation of professionals with our **off-the-shelf** or **tailored training programs**

COMPETENCES IN SEMICONDUCTOR PRODUCT DEVELOPMENT – NPI to VOLUME PRODUCTION



Turnkey, fixed-price solutions for several types of projects - enable **predictive schedule and budget planning**

INFRASTRUCTURE

DESIGN FOR TEST (DFT) – ENSURE TESTABILITY FROM THE START

EXPLORATION

- Feasibility studies
- Coverage analysis
- DfT architecture definition
- Memory BIST & repair strategy
- Fault model selection based on quality requirement
- Zero-Defect initiatives as per AECQ100
- Make vs buy decision for IPs
- Area vs Performance vs Quality trade-offs

IMPLEMENTATION

- Scan insertion, compression and diagnosis flow
- LBIST/IJTAG/JTAG/MBIST implementation
- Build memory repair and diagnosis flow
- Complete DFT flow implementation, verification and gate-level sign-off
- Familiar with a variety of products, IPs and SoCs

DEPLOYMENT

- Build and transfer development flows
- Train new engineers
- Write automation scripts (full IP ownership by clients)
- Documentation
- Tracking using client tools, Jira, Jama, Confluence, DOORS ..
- Functional safety compliance, ASIL A,B,C,D

Mentor Graphics (Siemens), Cadence, and Synopsys toolsets

BUILDING THE FOUNDATION FOR HIGH-QUALITY, COST-EFFECTIVE TEST SOLUTION

! A good design must also be easily and cost-effectively testable to be successful in the market

SILTEST can help with defining ..

Test Strategy — What needs to be tested, how and under what conditions – based on client objectives

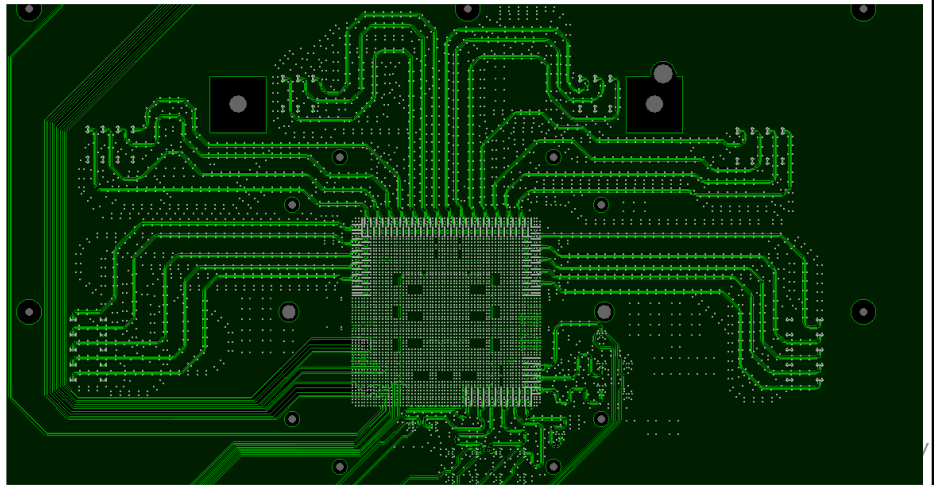
Coverage Goals — Coverage goals based on expected quality levels, and associated fault models

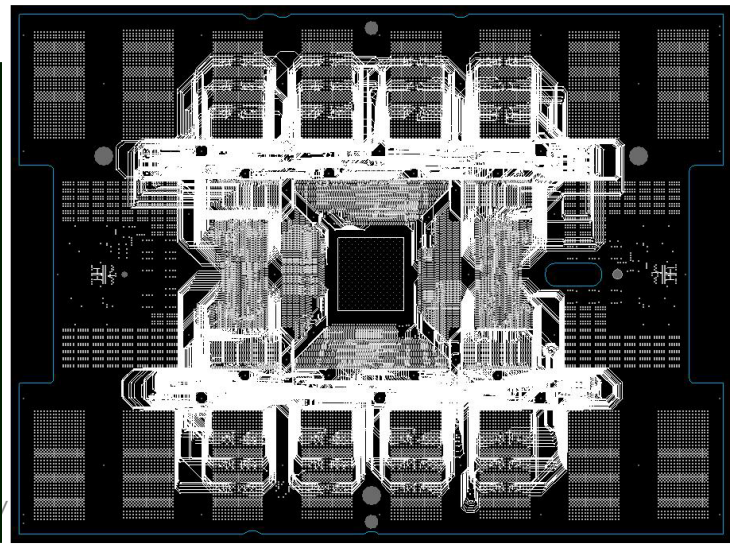
Test Flow — Optimum production test flow, various steps from wafer to burn-in to final to system level test

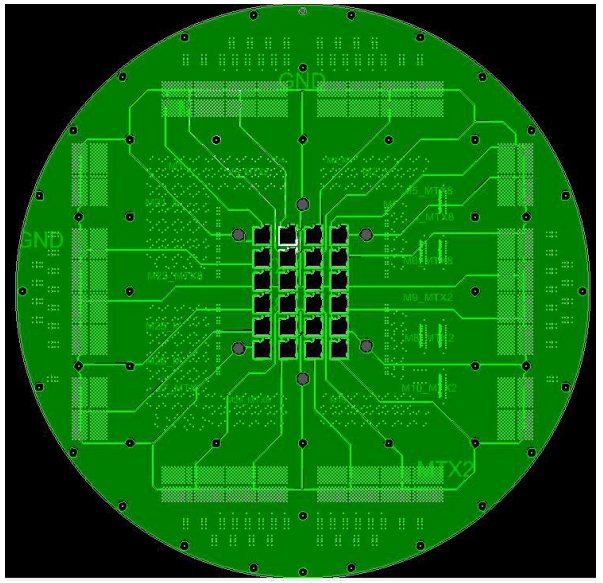
HARDWARE DESIGN – BOARDS FOR WAFER & FINAL TEST, QUALIFICATION, BURN-IN

We provide services in following areas:

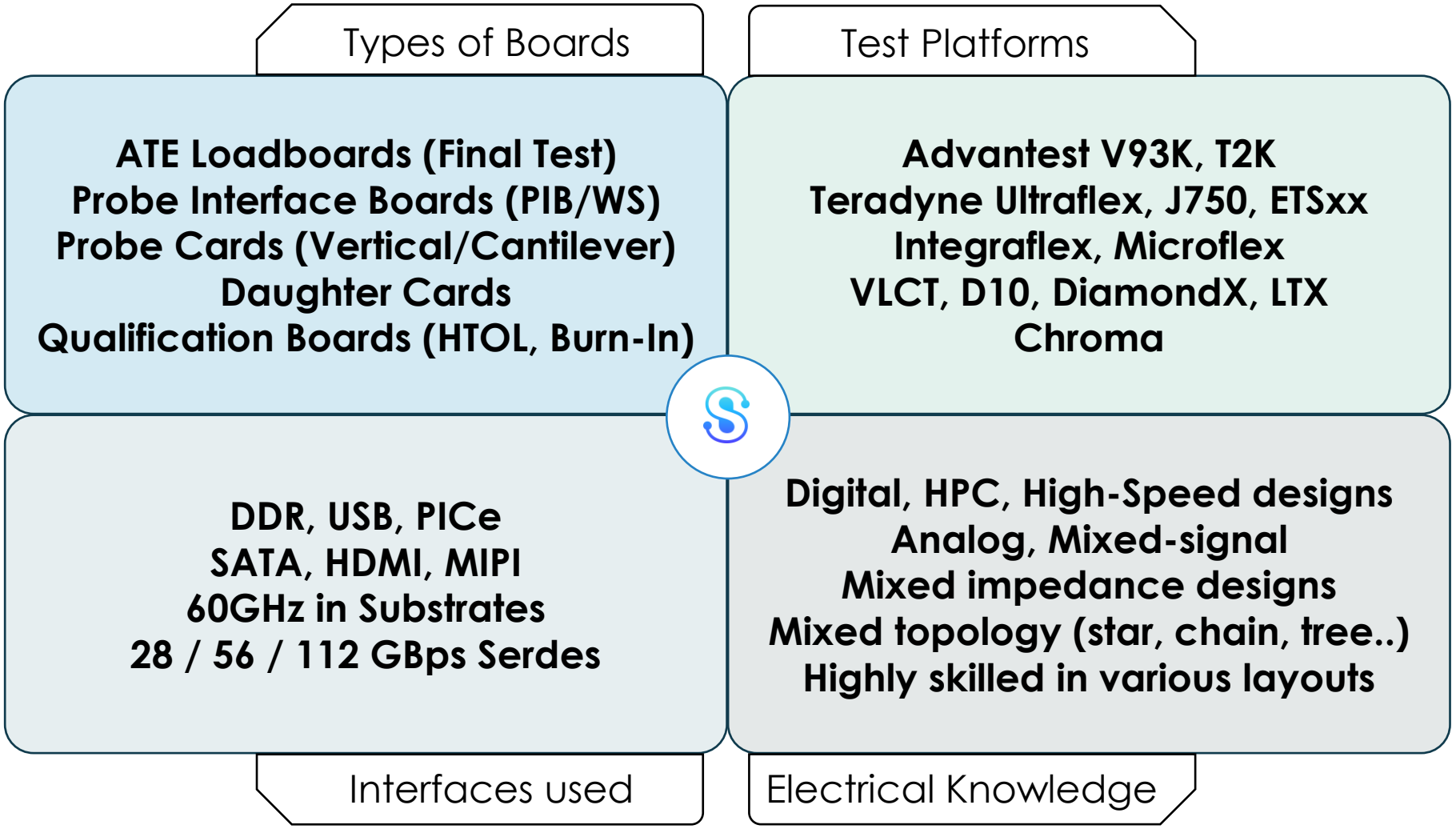
- ATE Test Interface board design: Load boards & Probe cards
- MLO / MLC Substrate design
- IC Package design
- Signal and Power Integrity simulation
- Library development and maintenance
- CAM Validation and Editing







HARDWARE DESIGN EXPERTISE



TEST ENGINEERING COMPETENCES

NPI

- Test methodology & strategy
- Test Plan creation
- Test Pattern generation, conversion
- Hardware development (WT/FT)
- Test Program (TP) development
- 1st Silicon bring-up
- Debug at Wafer and Final test
- Characterization, TP optimization
- Spike Check
- Automotive quality TP releases
- Expertise in Advantest 93K EXA Scale, SmarTest 8

SUSTAINING

- Test Platform conversion
- Multi-site conversions
- Wafer Fab transfers
- Qualifying new variants
- Test time improvements
- Code optimization
- Coverage updates
- Incremental releases
- Documentation and training

ALLIED SERVICES

Through our partners:

- Board assembly and manufacturing
- Software and firmware development
- Qual and reliability testing - ESD, Latch-up, Temperature cycling, HTOL/ELFR, manual probing, FIB..

Partnership and support from **Tester Companies**

TERADYNE (UltraFlex, J750, ETSxx), ADVANTEST (93K SMT**7**&**8**, T2K), LTX, NI-STS, Chroma

ADVANCED PACKAGING SERVICES

CAPABILITIES

- Semiconductor Package design and simulation services
- Small and mid-series assembly in an ISO7 facility (in European Union)
- Perfect setup for startups, small and mid-size companies
- Flexible and collaborative approach

PACKAGE TYPES

- WB-BGA (XFBGA) and FCCSP – 3x3 to 17x17mm
- Bare Die FCBGA – 7x7 to 21x21mm
- MCM and SiP
- Several QFN packages
- SOIC, QFP, DIP
- Ceramic – C-DIP, C-PGA..

INNOVATION

- Custom package design and qualification as per client needs
- Additional new packages in R&D stage, such as; Package-on-Package, Adaptive heat sink, Film Assisted Moulding, Exposed Die Lidded etc.
- Package quality and reliability assessment as per end-application and prevalent standards.

Packaging, Testing and Qualification Co-located to ensure efficiency

CHARACTERIZATION, QUALIFICATION, RELEASE

! Cool product idea is just the beginning, let's walk through essential steps to bring a product from Tapeout to Production (PPAP)

Packaging — SilTest will help you assemble your MPW/SPW wafer into samples of desired package

Engineering samples generation — Using bench setup or ATE, we will generate early engineering/customer samples

Enable Qualification — Generate test program with high-coverage to enable qualification and reliability testing

CONTINUED..

Run Qualification	Through our partners in Europe, we will execute all Qual steps, readouts and provide extensive reports
Characterization	Standard or matrix lot, we will execute thorough characterization across all operating conditions and provide reports
Release to Production	Finalize and release a cost-optimized test solution to enable high-volume production at chosen OSAT

We don't just stop here – SilTest supports clients in continuous **yield management** and **ongoing production activities**

PRODUCT & YIELD ENGINEERING COMPETENCES

NPI

- Knowledge in wide range of products – PMICs, Processors, High-speed interfaces, Transceivers, Data Converters. Power (SiC/GaN)
- Defining test and validation requirements
- Coverage gap analysis
- Process corner definition
- Supporting Qual and FA
- Characterization
- Supporting TE and other groups
- Yield and Quality target definition

SUSTAINING

- Yield improvements
- Wafer Fab transfers
- Hold lot releases
- Quality improvement (ppm)
- Drift analysis, gauge R&R, bin-flip analysis
- HW and SW correlations
- HW releases
- TP update releases
- Reporting and documentation

INNOVATION

- Co-develop tools for client needs using AI/ML
- Advanced AI techniques to improve yield and quality
- AI image processing to accelerate Si level debug and FA
- Automate and create simplified processes
- Standard test solutions for common ICs to enable MCMs and Chiplets

Several process technologies from TSMC, GF, Intel and Multiple Tester Platforms

YIELD MANAGEMENT – FROM NPI TO VOLUME PRODUCTION

SilTest in-house tool, **YieldOptiX** packs several Machine-Learning enabled features to simplify NPI development.

Our partnership with **yieldWerx** is powerful way to scale yield management into volume production:

- Yield-improvement: SilTest will evaluate optimization potential, commit to yield improvement on a **results-based compensation** model
- Cost-optimization: in our experience, there is a **15-30% cost optimization** possibility across large product portfolios
- Quality-improvement-as-a-service: implementation of **PAT/DPAT/DeepLearning** and other advanced techniques to improve ppm

See how our Yield Management solution scales with various stages of product development →

- YieldOptiX
- yieldWerx

Test Program (from first data log)

(Built-in STDF parser, Dynamic Filtering, Limits Comparison, Tests-to-Blocks Grouping)

- Test block coverage validation
- Easy check for per-block test completeness
- Convenient test name convention checks
- First plotting templates design
- Plotting plan shareable with other projects and teams

Qualification

(Excel exports, Drift Analysis)

- Convenient fail pattern assessment via color-coded Excel exports
- Drift analysis and trends evaluation

Ramp-Up

(GRR, Root Cause Analysis, Lot Release)

- Instant test program and hardware releases via Gauge R&R
- ML/AI-driven root cause analysis for bins and fail patterns
- Interactive correlation analysis
- Lot release with dedicated ink-off module
- Bin flip evaluation for test time optimization

Characterization

(Automated Reporting, Efficient and Scalable Visualizations)

- Easy creation of complex plots with automation
- Ultra-fast, comprehensive statistical summaries
- Outlier detection with retest scenario evaluation
- Custom naming and multi-level X-axis support

Bring-Up

(Automated Reporting, Interactive Pareto Charts, Maps, Limits Setup)

- Automated reporting by test block using custom/shareable templates
- Easy grouping of multiple tests into a single chart
- Deep-dive into data with highly customizable plots
- Full interactivity for live data exploration
- Limits setup: custom or calculated with adaptive rounding
- Yield by test block analysis (in "continue on fail" mode) and yield simulations
- ML/AI clustering for failing test detection
- ATE to bench correlation support
- Structured data sharing via color-coded Excel exports

Production

(Lot release, Fail Cluster Analysis, Field Return Investigations)

- Lot release module supporting both parametric and geometric ink-off
- Detection of recurring fail clusters across production lots
- Context analysis beyond individual tests – exploration of patterns across multiple measurements, parts, or lots
- Intelligent Excel exports to support filed return analysis

ACCESS TO ADVANCED TEST FLOORS 🇩🇪🇳🇱🇫🇷

SilTest has access to state-of-the-art test floors, with latest equipment as listed

<table>
<tr>
<td rowspan="2">ATE Equipment

• 10x Advantest V93k
• 8x Teradyne UltraFLEX, w/ RF, HexVS and VMS
• 1x Teradyne FLEX-RF & µFLEX
• 3x Teradyne J750 with 1024 channel head
• 1x Teradyne ETS-88
• 1x Chroma 3680
• 1x Chroma 3650-S2 (GaN/SiC testing)</td>
<td>Wafer Probers (20° to 150°C)

• TEL P–12XLm for 6, 8 & 12“ wafers
• TSK-UF200 for 6 and 8“ wafers</td>
</tr>
<tr>
<td>Device Handlers (-60° to 150°C)

• Chroma 3160C production (3 temp.)
• ESMO Talos engineering (3 temp.)
• Exatron 903 engineering (3 temp.)

Thermostreamer
• Thermonics T-2500E</td>
</tr>
<tr>
<td colspan="2">Characterization Equipment: Several basic lab instruments, oscilloscopes, and Applicos ATX7006A for ADC/DAC bench testing</td>
</tr>
</table>

CONTACT

SilTest Semiconductors GmbH
Boschstraße 16, 47533 Kleve. Germany

Email: info@siltest.com

Sameer Saran
sameer.saran@siltest.com

Mike Bartley
mike@alpinum-consulting.com