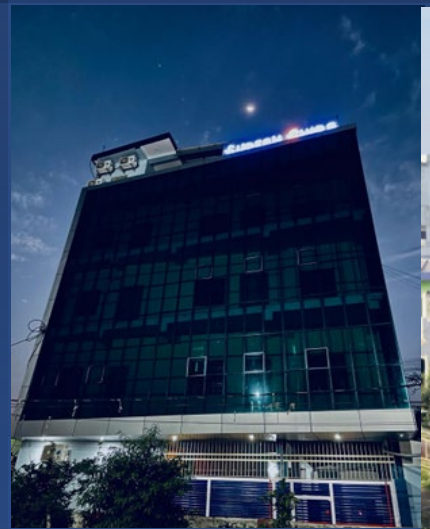
Overview

SURESH CHIPS
& Semiconductor



Vision and Mission

SURESH CHIPS & Semiconductor

Vision

"Suresh Chips & Semiconductor envisions becoming a responsive, AI-driven partner, ensuring high quality and agility in meeting ever-evolving technology needs of our customers."

Mission

"Suresh Chips & Semiconductor endeavors to develop pioneering technology service platforms that seamlessly integrate human intelligence with artificial intelligence. We're committed to being a responsive, high-quality partner, evolving alongside our customers' dynamic technology needs."

Expertise

- Design and Verification
- Physical Design
- Analog Circuit Design and Layout
- SIGN-OFF Expertise
- Test Solutions and Services(DFT)
- Embedded System & Controls

Expert Technical Leads who drive the competency in each of the design verticals

Key Differentiators

SURESH CHIPS & Semiconductor

❖ Leadership Team with Pedigree and Proven Track record

- Seasoned leadership team with average Experience of 15+ Yrs.
- Wide domain expertise in end-to-end IC development in product companies
- Execution and Team building track record

❖ Access to globally top-notch expert consultants

- Advisory Board to comprise of internationally recognized technical experts
- Association with top business leaders with proven track record

❖ Ability to leverage top tier national academia

- Access to top tier talent (IIT/IISc)
- Incubate product ideas from cutting edge research

❖ Longer runway to hit critical mass

- Long term past association being the foundation of trust and cohesive decision making

Leadership Team Snapshot

Chandan Raj

- CEO and Founder of Suresh Chips and Semiconductor
- 16 years of work experience in companies like Intel, Samsung, Nokia and AMD
- Semiconductor Product Development Methodology
- Product Architecting and Ramping to Market
- Trained and Built Highly Skilled Design Teams which Delivered Products for Global Market

Kundan Raj

- Co-Founder and CTO of Suresh Chips and Semiconductor
- 15 years of work experience in companies like Synopsys, NXP, Mediatek, Analog Devices, Samsung and AMD
- Deeply involved in leading a team that excels in ASIC, FPGA, and mixed-signal design and verification

Leadership Team Snapshot

Mike Bartley

- Board Advisor of Suresh Chips and Semiconductor
- 37+ years of experience in software testing and hardware verification
- Built and managed state-of-the-art test and verification teams inside several companies (including STMicroelectronics, Infineon, Panasonic, and the start-up ClearSpeed) and also advised several companies on organisational verification strategies (ARM, NXP, and multiple start-ups).
- Successfully founded and grew a design services company to 450+ engineers globally, delivering services and solutions to over 50+ clients in various technologies and industries

Han Xuming

- Technical Manager of Suresh Chips and Semiconductor
- 25 years of work experience in companies like Huawei Technologies, Nokia, Bell Labs
- R&D team lead and management experience in Functional and Formal verification
- Managing Front-end teams in China with multiple clients

Our Office

SURESH CHIPS & Semiconductor

❖ State-of-the-Art Infrastructure

Equipped with high-speed internet, modern workstations, and the latest technology to ensure seamless operations

❖ Collaborative Spaces

Open-plan areas designed for team brainstorming sessions, along with private meeting rooms for client interactions and confidential discussions

❖ 24/7 Security and Access Control

Secure premises with surveillance cameras, biometric access, and round- the-clock security for a safe working environment

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DESIGN & VERIFICATION EXPERTISE

Design

- Micro Architecture
- RTL coding & SoC Integration
- Linting, CDC, formal for Low Power
- Synthesis, Logic equivalence

Verification

- Constrained Random Verification
- Assertion based Verification
- Coverage Driven Verification
- Formal Verification
- Power Aware Verification
- AMS Verification

Protocols

- PCIe, Ethernet, Ethercat, ONFI, CXL, USB
- AMBA AXI, ACE, AHB, APB, ATB, ATP, GFB, OCP, SPMI, DDR, LPDDR, MIPI, SPI, I2C, I3C, CXS, UART, WDT
- Image processing and Video codecs, LTE signal chain, Viterbi and Turbo decoders, baseband functions, UPF

Methodology/ Tools/Languages

- UVM, OVM, VMM, eRM, RVM
- VCS, Questa, IES, Simvision, Verdi, Vplanner, Emanager, CDC, Spyglass, MVRC, Conformal LP, DC, LEC, Formality, PT, RTL Encounter, Fastscan
- Verilog, System Verilog, C, C++, SystemC

PHYSICAL DESIGN EXPERTISE

Synthesis

- DC/RTL Compiler
- Physical Aware Synthesis
- Low Power Aware
- DFT insertion
- Logical Equivalence

Pre/Post STA

- Timing budgeting at SOC
- Constraints Development
- IO timing closure
- Timing ECO generation
- SOC / Subsystem Timing closure

Placement & Route

- Floor planning and Partitioning
- Clock-Tree Synthesis
- Multi-Mode Multi-Corner Opt
- Power Optimization
- High Utilization
- UPF/CPF aware flows

Sign-Off

- Hierarchical Designs
- Flat STA closure
- Physical Verification
- IR and EM checks
- SOC Low Power checks
- SI and PI

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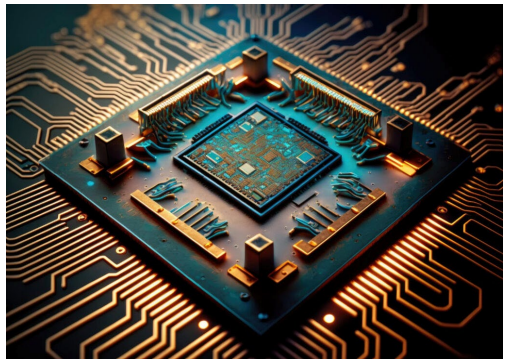
DFT EXPERTISE

DFT

- Scan Insertion
- ATPG
- Test pattern generation and simulation
- Coverage improvement
- IDDQ
- BIST
- BSCAN
- DFT Spyglass checks
- Test mode timing constraints



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Analog Design/Layout EXPERTISE

ASIC DESIGN

- Custom Chip
- Mixed Signal Integration
- Low Power Design
- High Frequency

Analog Design

Analog & Mixed Signal Layout

- SOC Integration
- PLL
- DAC
- ADC
- CLOCK SYNTHESISER’s

CUSTOM LAYOUT

- Analog routing
- Memory layout
- Standard cell
- Custom Digital

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SIGN-OFF EXPERTISE

PDN

- IR Drop Analysis.
- EM analysis.
- Rush Current Analysis.
- Generating EM-IR models.
- Defining EM-IR flows & Sign-Off methodologies

FEV &. VCLP

- Static Low power checks at SOC / Subsystem / Block level.
- Power Intent Verification at Designs
- Logical Equivalence checks - RTL to RTL , RTL to Netlist & Netlist to Netlist
- Low power enabled Equivalence checks

DRC & LVS

- SOC level DRC and LVS checks
- PERC checks
- Electrical Checks
- ESD checks

Expert Technical Leads who drive the competency in each of the design verticals

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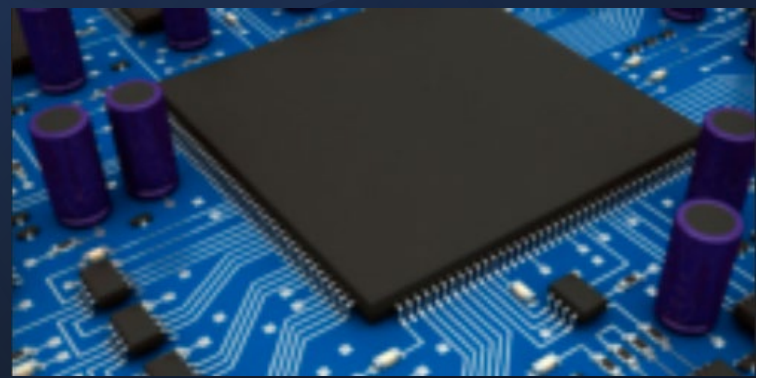
VIP and EDA PRODUCTS



VIP Products

❖*Functional VIP*

❑AMBA
- AXI
- AXI Stream
- AHB
- APB

❑TCM

❑JTAG – First in the industry with openOCD

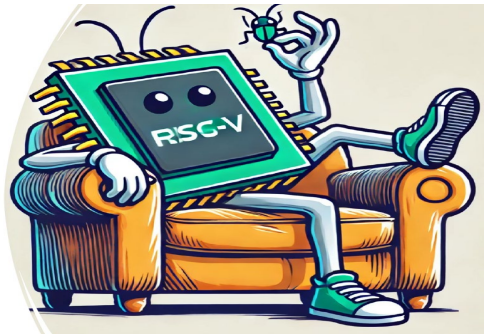
❖*Formal VIP*

❑RISC-V

❑AXI

❖*EDA Tool (Simulator)*

❑ Formal RISC-V (Developing)



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Successfully Executed Projects

AMD	Navi31, Navi32, Navi33, Navi36, Navi3C, Navi44, Navi48, Navi4C, Navi4X, MI200, MI300, MI350
INTEL	ACR CPP, FM4, FM7, FP8, SM7
Google[GChips]	Laguna, Malibu

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Client: AMD

Project Navi31, Navi32, Navi33, Navi36, Navi3C, Navi44, Navi48, Navi4C, Navi4X, MI200, MI300, MI350

Work Done by us

- RTL Design
- Functional Verification
- Formal Verification
- Emulation
- Design For Testability
- Physical Design
- Analog Circuit Design
- Analog Layout

Project Duration 48 months

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Client: Intel

Project ACR CPP, FM4, FM7, FP8, SM7

Work Done by us

- RTL Design
- Functional Verification
- Formal Verification
- Design For Testability
- Physical Design
- Analog Circuit Design
- Analog Layout

Project Duration 42 months

Client:Google

Project Laguna, Malibu

Work Done by us

- RTL Design
- Verification
- Design For Testability
- Physical Design
- Analog Circuit Design
- Analog Layout

Project Duration 28 months

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THANK YOU !!!

info@schipsemi.com

https://schipsemi.com/

Located @Muzaffarpur (Bihar, INDIA)

Contact Us: +91-9538479368