# Accelerating FPGA prototyping bring-up time

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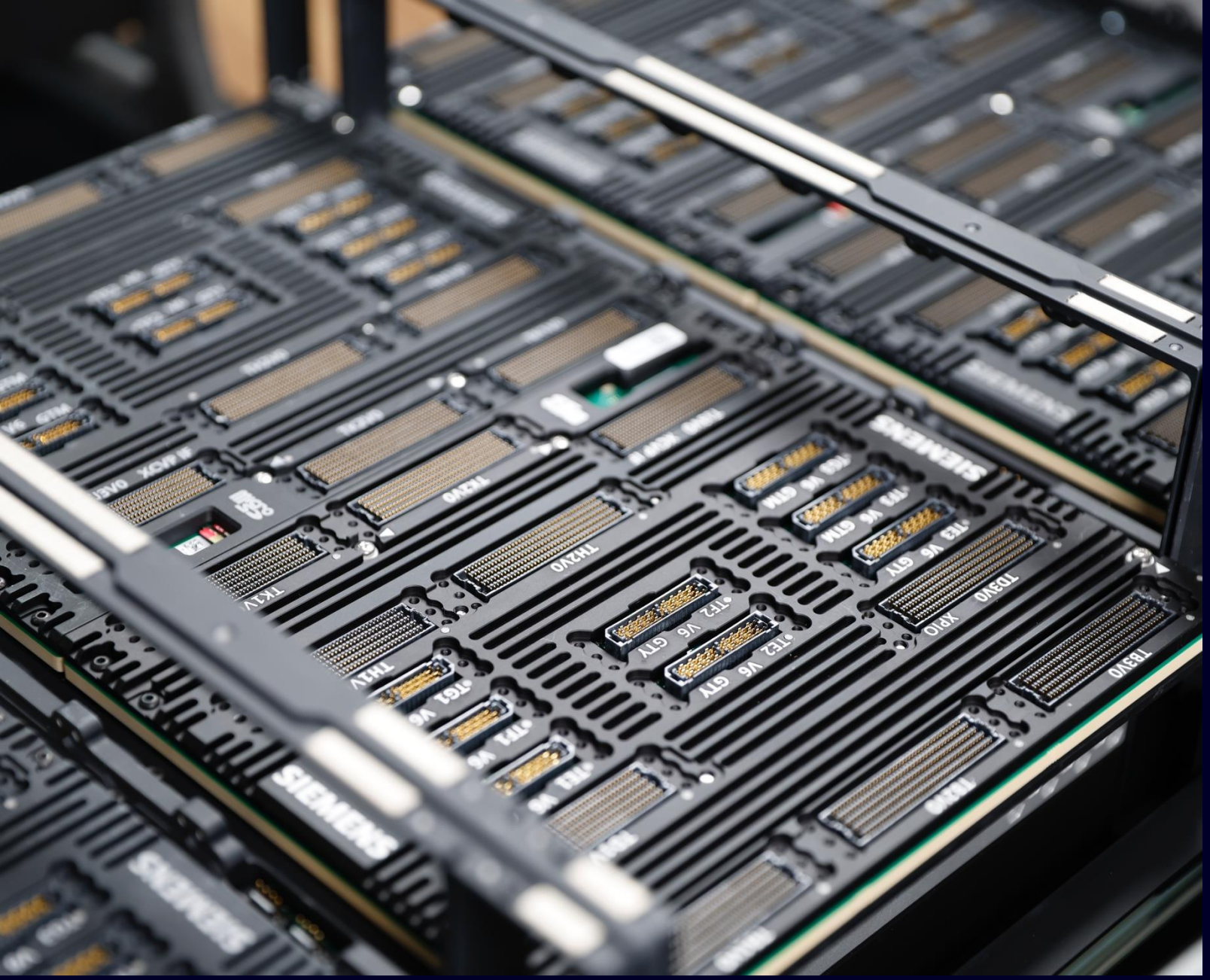


# Agenda

**3-phases for prototypes bring-up**

**Compile flow**

**Runtime**

**Debug**

**VPS and proFPGA CS**



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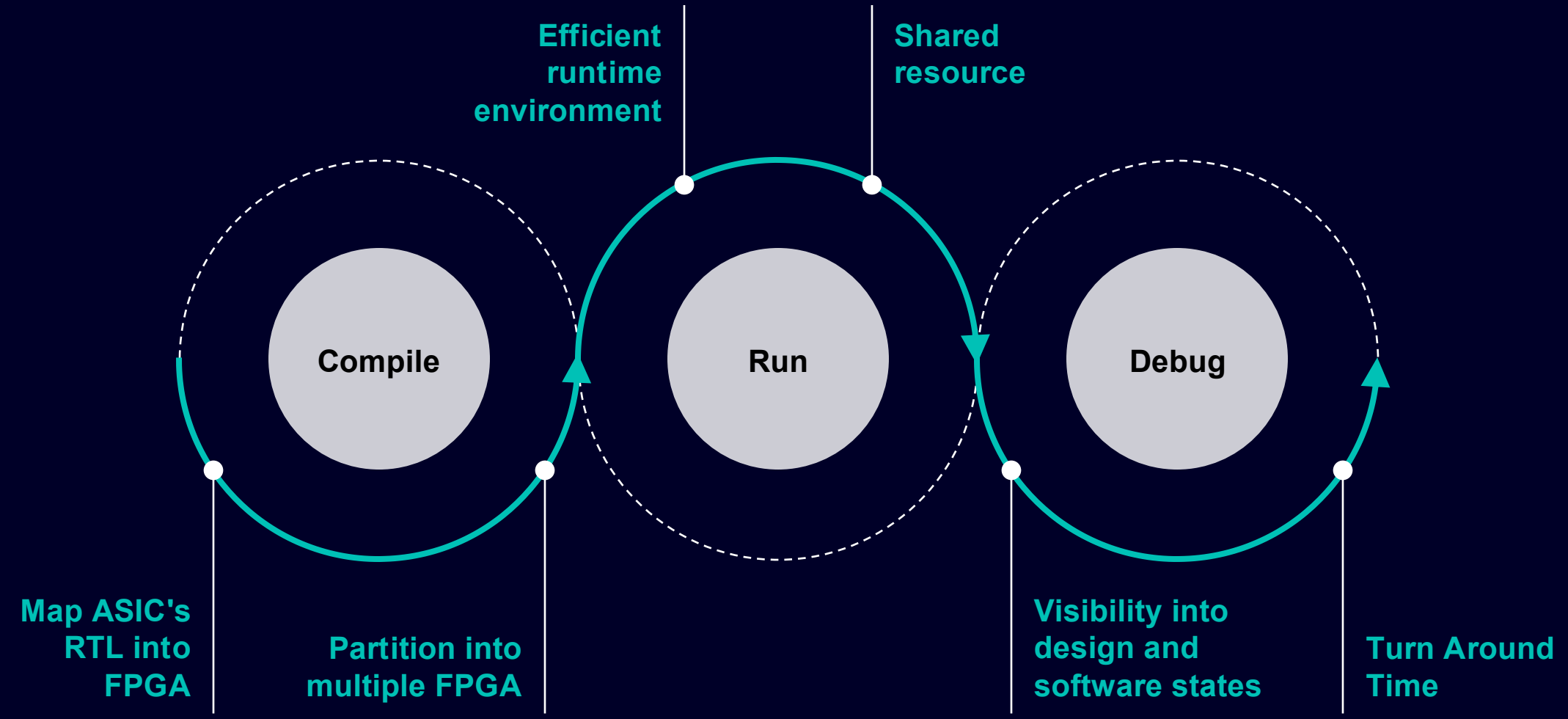
# The 3 phases for deploying a FPGA-based prototype system



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# Why commercial prototyping software ?

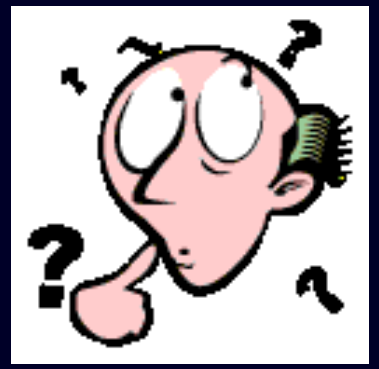
**ASIC and FPGA architecture mismatch**
IP and architectural structures don’t map directly

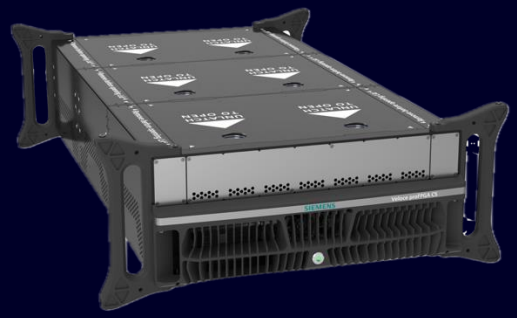
**Lack of Automation** & reproducibility
Manual processes lead to error and inconsistent results

**Timing closure and Performance**
Time consuming iterative process to get optimal results

**Protocols** integration complexity
Increase debug time and could penalized ease of use

**Design complexity & Debug challenges**
Will my implementation still be functional ?







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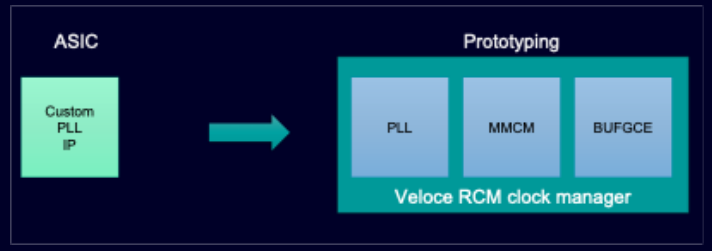
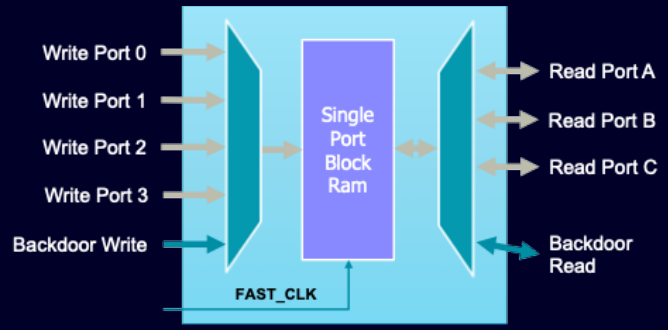
# FPGA bring-up automation

**Clock tree**
FPGA Clock module
Gated clock conversion
Clock distribution engine




VPS SW

**Design memories**
Auto-memory inference
Handling external memory
SoftModel




**FPGA partitioning**
Automated to customer constraints
Efficient bring-up and best performance



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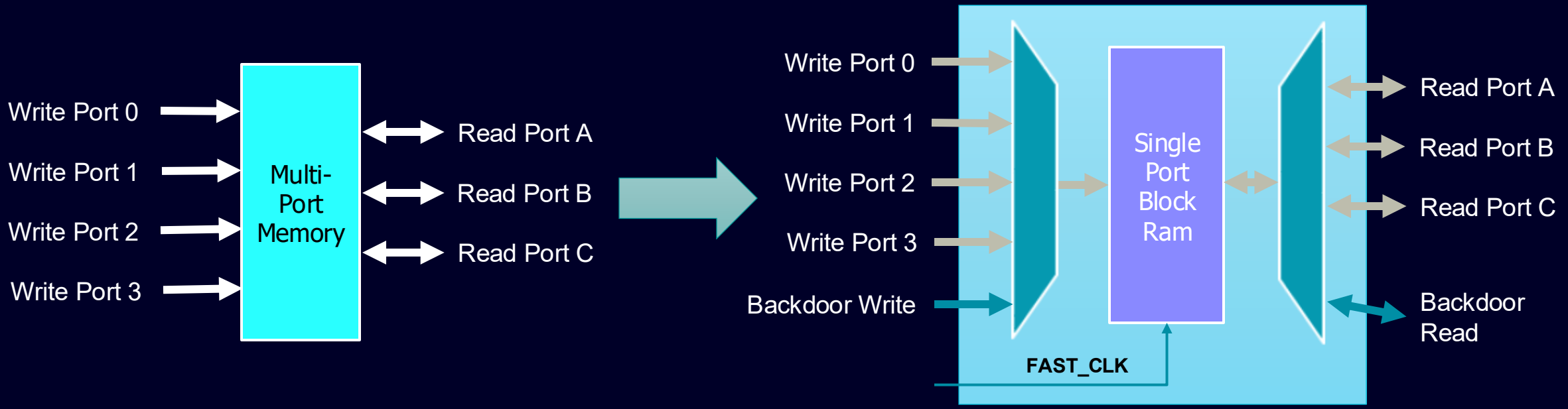
# Minimal RTL modification – Memory

Custom/internal memories in RTL are **automatically mapped** to FPGA memory resources

**Large memories** mapped into multiple FPGA or **external memory board**

**Memory Softmodels** available for HBM, DDR5, Flash memories

VPS SW enables **flexible mapping to FPGA primitives**



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# Multi-FPGA partitioning technics

## 1 Manual Partitioning

- User directives honored
- Cabling from user
- Auto pin muxing
- Auto debug instrumentation
- FPGA Wrapping

## 2 Automatic partitioning

- Auto Cabling
- Interconnect for best performances
- User can provide guidance

## 3 Hybrid partitioning

- Optimized implementation
- Customized prototype with best performance
- leveraging user experience



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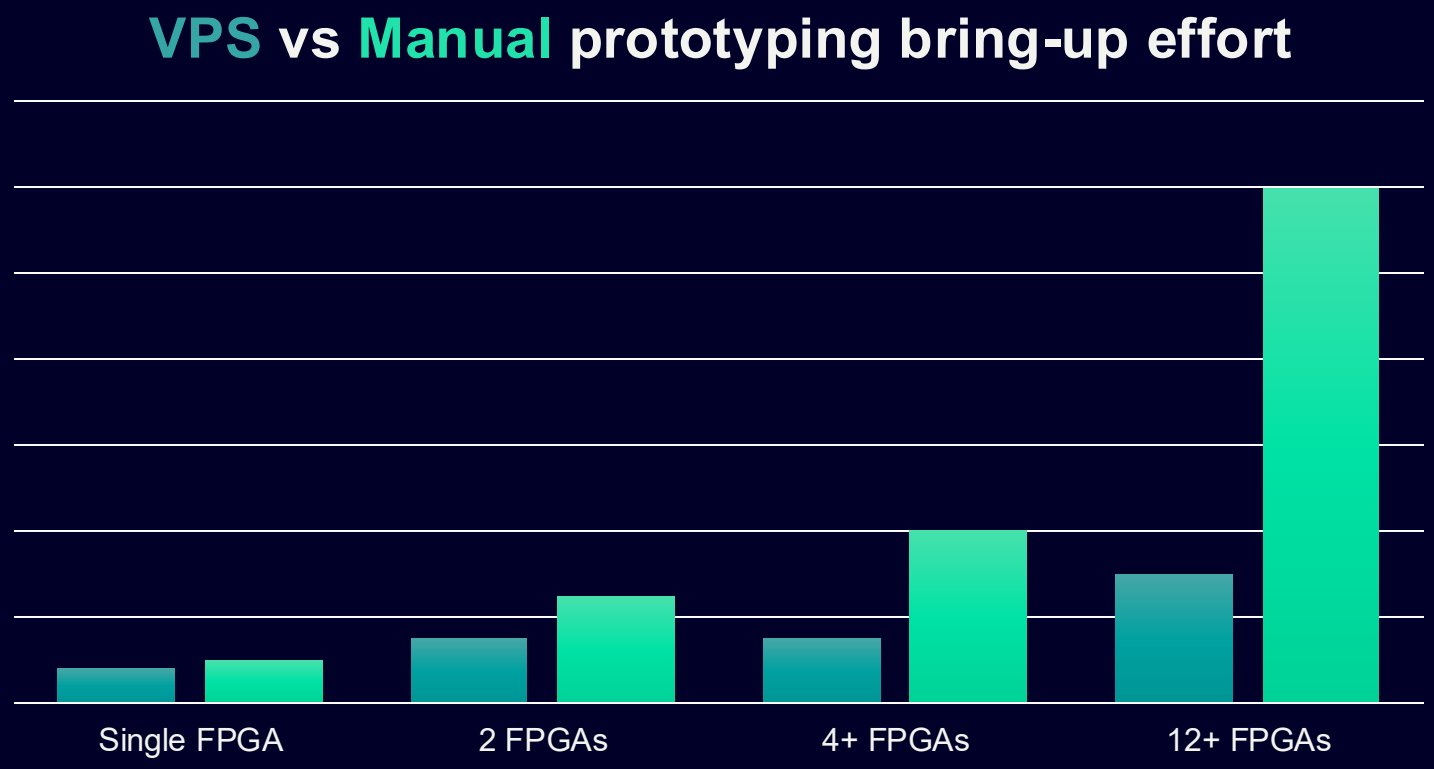
# VPS reduces time to prototype

**Single FPGA**

Benefits from memory compilation and clock management

**Multi-FPGAs**

Making the impossible possible, in a short amount of time



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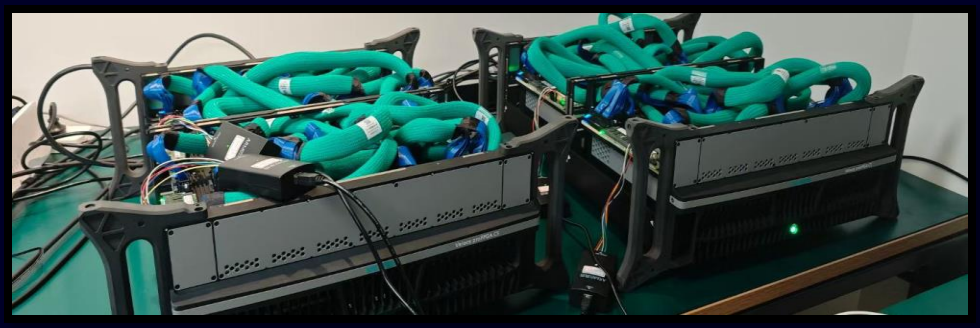
# From Desk to Datacenter

Use **same bitstream** on a **Desktop platform** or in a **FPGA Farm**

**Multi-user** and **Multi-project** hardware setup

**Efficient** deployment of thousands of FPGAs

Host **controlled** or **Standalone**

Network


Farm of FPGAs



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# Advanced debug capabilities

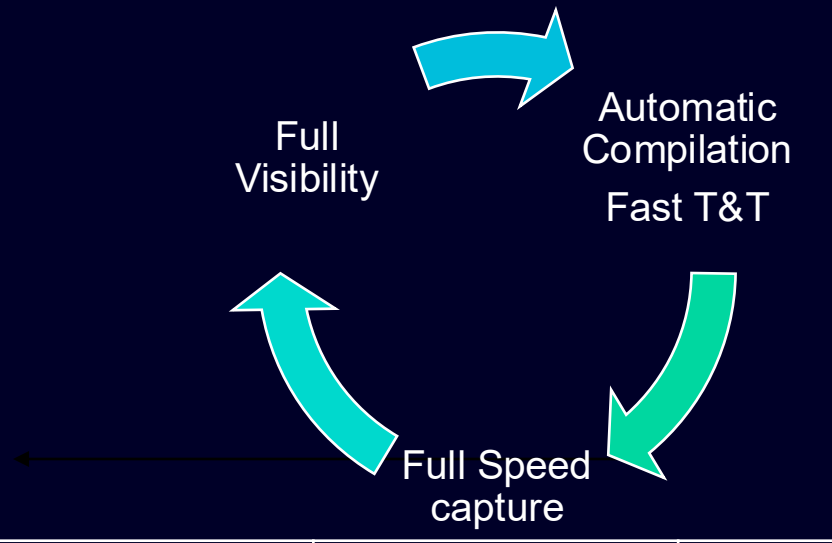
**Probed Debugging at RTL or Netlist level**

**Probe-less Debugging & Full Visibility at no capacity overhead**

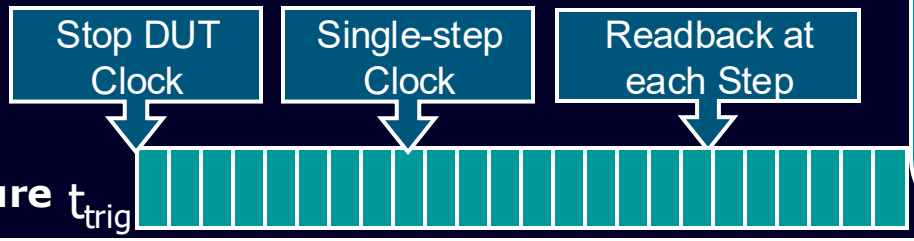
**Trigger on HW event**

**Streaming to DDR or to external Host**

**Same Waveform Viewer across all HAV products**




| Compile Frontend | Runtime Speed | Waveform generation |
|---|---|---|
| | 10+MHz | 100k Cycle in 20min |




Concatenate Data to Create Waveforms



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# Siemens' Veloce proFPGA CS platform

## UNO Desktop

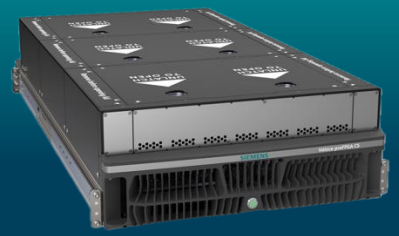
Single FPGA board

100+MHz

## QUAD/HEXA Desktop

Multi-FPGA Multi-user

## HEXA Blade



Data-center standard

Remote management

## Multi-blade System


Billions gates designs

Enterprise solution

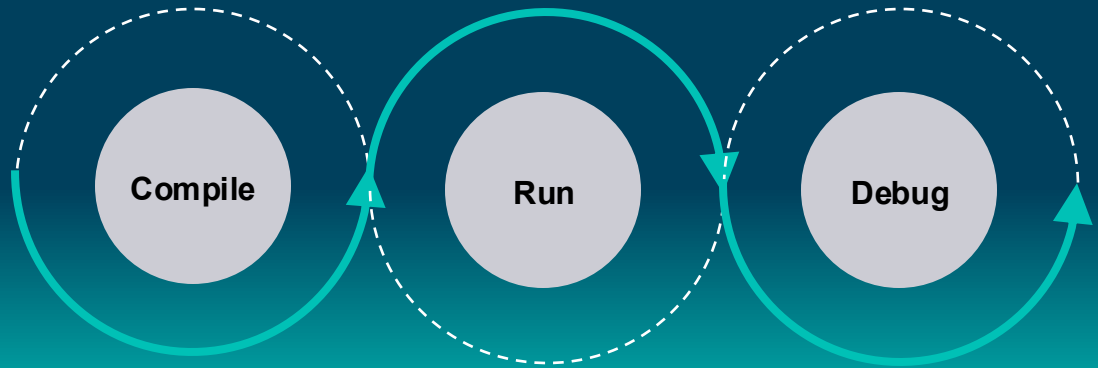
AMD VP1902

**Same functionalities across all HW**

**Minimal** RTL **change**

**Automatic** partitioning

**Automatic** cabling




**Standalone** or **Host** controlled

Runtime **efficiency**

**Advanced Debug**



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# Contact

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