

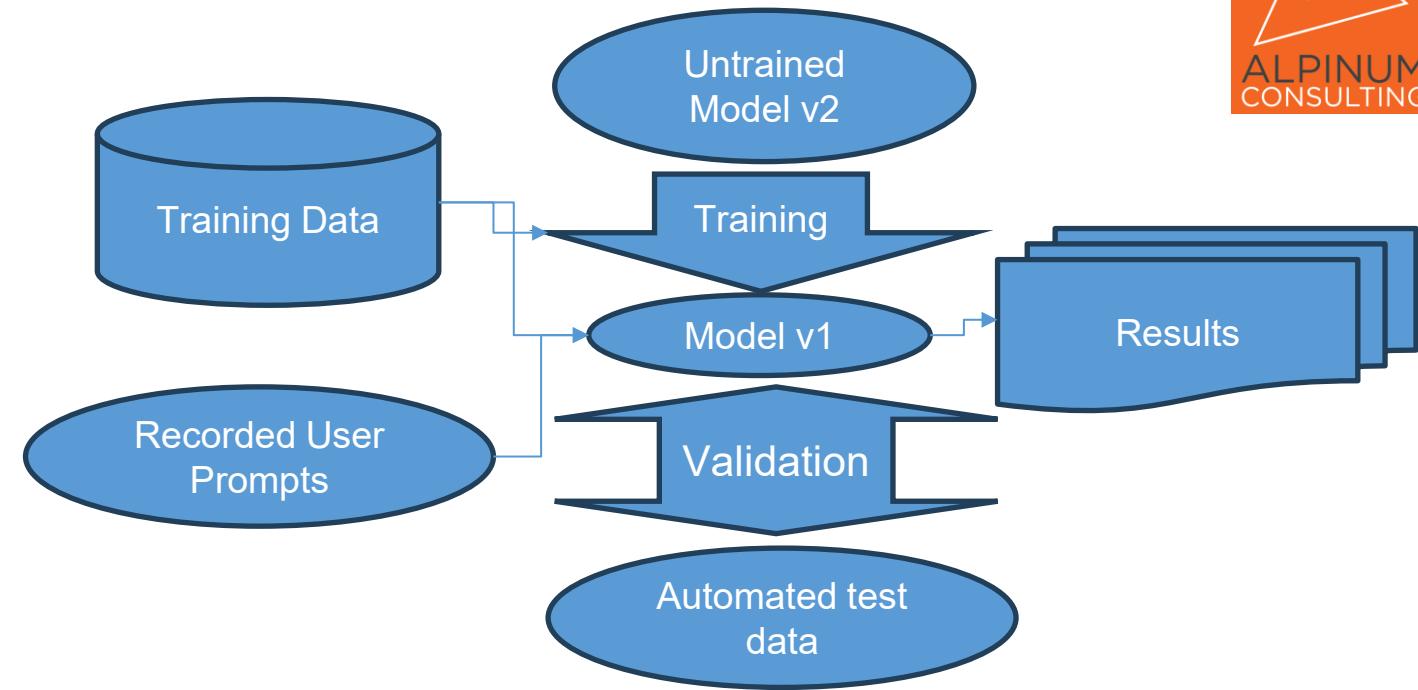
# AI in Design Verification

**Mike Bartley**, CEO, Alpinum Consulting

- Infrastructure and security
- Deployment for Design Verification at Tessolve
- Automating generation for UVM test benches, tests, coverage and debug

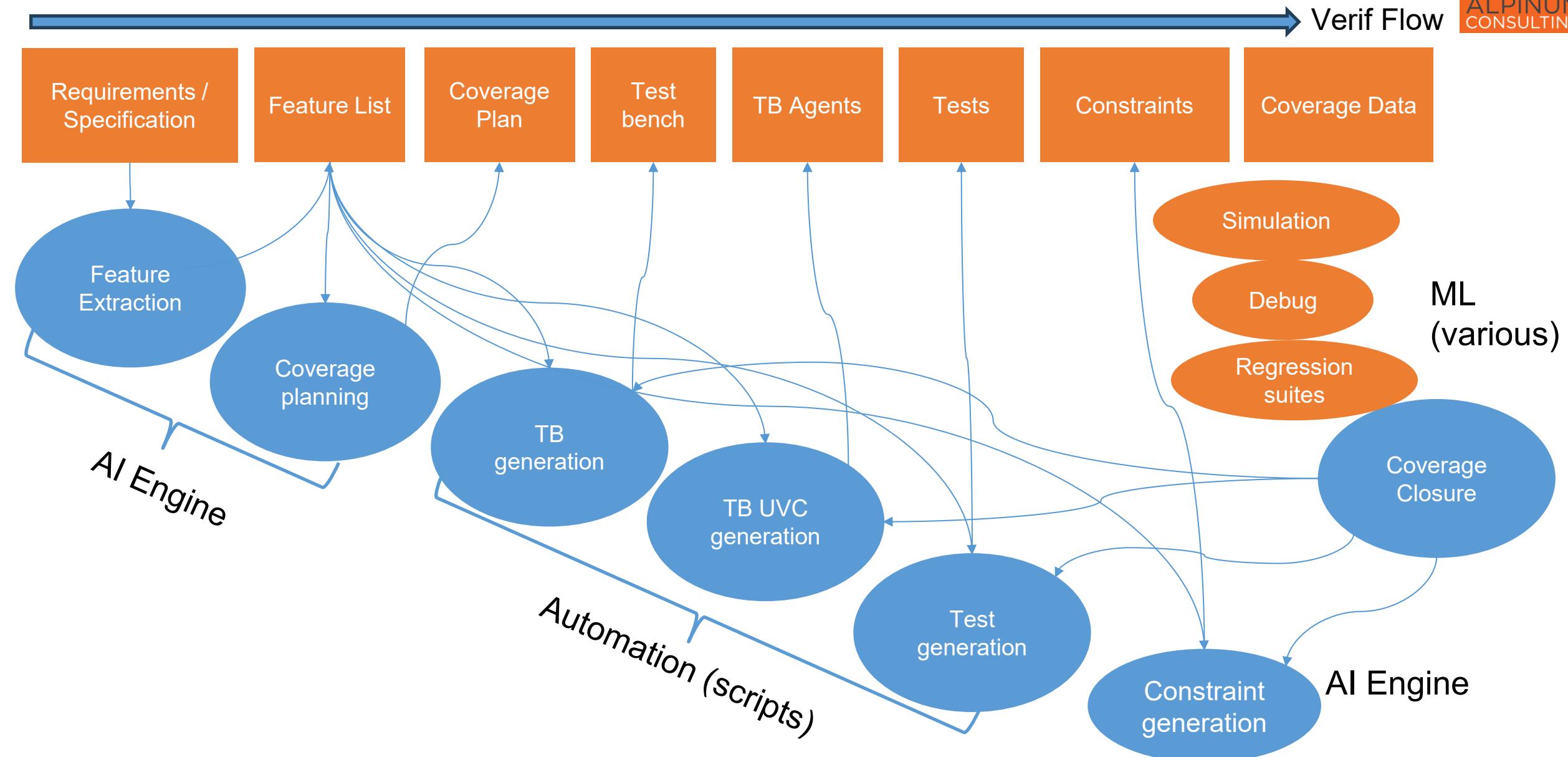
# Effective AI Strategy

- Central AI services:
  - Services/Guidance/reviews
- Central SW services
  - SW dev services



- **Models are replaceable**
  - Ensure training data is stored
  - to re-train new model releases
- **Maintaining security**
  - Different infrastructure for various security needs
- **Centre supports innovation at the edge**

# AI/ML automation in IP Verification



# AI Ecosystem

## Knowledge Bots:

- **Features:** Faster to develop & deploy
- **Use case:** With less confidential data, Project CoPilot
- **Security:** Low
- **Cost:** Low
- Reasonable accuracy,
- **Project:** UVM Chatbot, FUSA Chatbot

## Build: Cloud Deploy: Cloud/ Hosting Services

- **Feature:** Faster develop & deploy
- **Use case:** Client projects, highly confidential data.
- **Security:** High
- **Cost:** High

## Build: Local Deploy: Local

- **Features:** Slower to develop & slower to deploy
- **Use case:** For highly confidential data
- **Security:** High
- **Cost:** High
- **Challenge:** Less Adaptability, less Scalability, Upfront Cost

## AI Apps

- DV Spec Analysis Tool
- DV AI TB Tool
- Assertify Tool
- Domain/ Project based AI models
- PDK AI Training Tool
- AI Code Copilot

# 1: UVM AI Training Tool

## Organized Content

- Follows planned flow

## Quick Topics

- Most important topics' explanation

## MCQs

- Test, Evaluation, weak concept suggestions

## FAQs

- Clarifies on common important doubts

## Q&A

- ANY question support

## About

- Tool briefing for effective use

## Benefits:

- Self guided and self paced flow
- Analytics & custom topic suggestions
- Ask anything about UVM
- Improved accessibility
- Reduced training time
- Scalable for other domains

# 1: UVM AI Training Tool

Welcome, marmik soni!

Logout

---

≡ Navigation

- Organized Content
- Quick Topics
- Generate MCQs
- Top 10 FAQs
- Q&A Chat**
- Chat History
- About

**TESSOLVE**  
A HERO ELECTRONIX VENTURE

## Tessolve UVM AI Training Tool

### Q&A Chat

 Explain UVM Sequencer please!

# UVM Sequencer

## Introduction

In Universal Verification Methodology (UVM), the sequencer is a key component responsible for controlling the flow of sequences that generate complex stimulus and the drivers that convert these stimuli into pin-level activities.

## Role of the Sequencer

 Developed by AI CoE team

# 1: UVM AI Training Tool

Welcome, marmik soni!

Logout

## ☰ Navigation

☰ Organized Content

⚡ Quick Topics

✍ Generate MCQs

ⓘ Top 10 FAQs

💬 Q&A Chat

🕒 Chat History

ⓘ About



## Tessolve UVM AI Training Tool

### ✍ Generate MCQs

Select a topic

UVM Components

Generate MCQs

### MCQs for UVM Components:

Question 1: What is the primary class from which the `uvm_component` class inherits?

Select an option:

- (A) `uvm_report_object`
- (B) `uvm_sequence`
- (C) `uvm_driver`
- (D) `uvm_monitor`

Question 2: Which of the following `uvm_component` classes encapsulates sub-components for sequence communication with the `uvm_driver`?

Select an option:

- (A) `uvm_subscriber`



Developed by AI CoE team

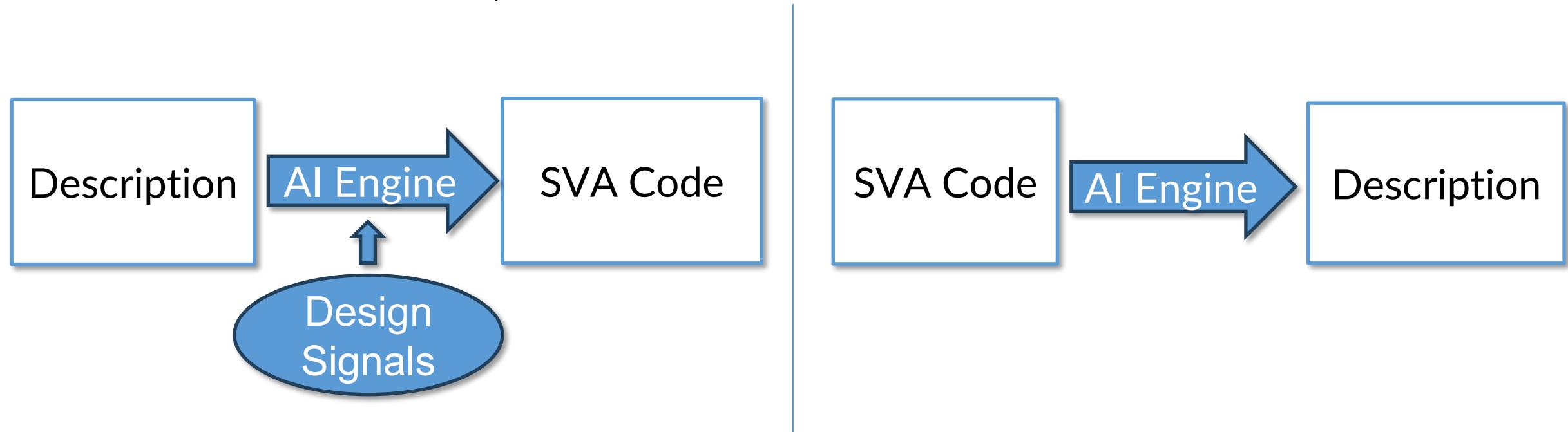
## Tool 2: Assertify Tool

Problems around Assertions are:

- | Growing Complexity in Verification
- | Human Errors
- | Time intensive asks
- | Lack of Consistency and Skill Gap

Use case:

1. Generate Assertions from spec/ engineer's simple description using AI models.
2. Generate description from the SVA code.



## Tool 2: Assertify Tool - Signal match analysis

#	Approach	Top signal	Assertify tool input english description signal	Signal in generated SVA
1	Case mismatch	axi_awvalid	AXI_AWVALID	axi_awvalid
		axi_awready	AXI_AWREADY	axi_awready
2	Additional character	axi_awvalid	AXIVALID	axi_awvalid
		axi_awready	AXIREADY	axi_awready
3	Partial match	axi_awvalid	AXIVLD	axi_awvalid
		axi_awready	AXIRD	axi_awready
4	Partial match	axi_awvalid	valid	axi_awvalid
		axi_awready	ready	axi_awready
5	Highly mismatch	axi_awvalid	VLD	axi_awvalid
		axi_awready	RDY	axi_awready

# Tool 2: Assertify Tool

Upload TOP Level PDF File:

Choose a PDF file

?

Drag and drop file here

Limit 1GB per file • PDF

Browse files

 axi\_top.pdf  
36.7KB

X

## SystemVerilog Assertion to English

SystemVerilog Assertion Code

?

```
systemverilog
property awvalid_protocol;
  @(posedge clk) disable iff (!rst_n)
    axi_awvalid |>##[1:$] axi_awready;
endproperty

assert property (awvalid_protocol);
```

Convert to  
English

Code Description

?

The SystemVerilog assertion `awvalid\_protocol` checks that whenever the axi\_awvalid signal is asserted (indicating that the write address is valid), the axi\_awready signal must be asserted at some point in the future, ensuring that the write address handshake is completed. This must hold true on every positive edge of the clk signal, provided the rst\_n signal is not asserted (i.e., the system is not in reset).



# Tool 3: Spec Extraction Tool

- RAG (Retrieval Augmented Generation) Tool for DV Spec Extraction
  - Inputs: Project Spec, Training Data, Prompt (Character)
  - User Prompt
  - LLM Intelligence
  - Output

## Flow

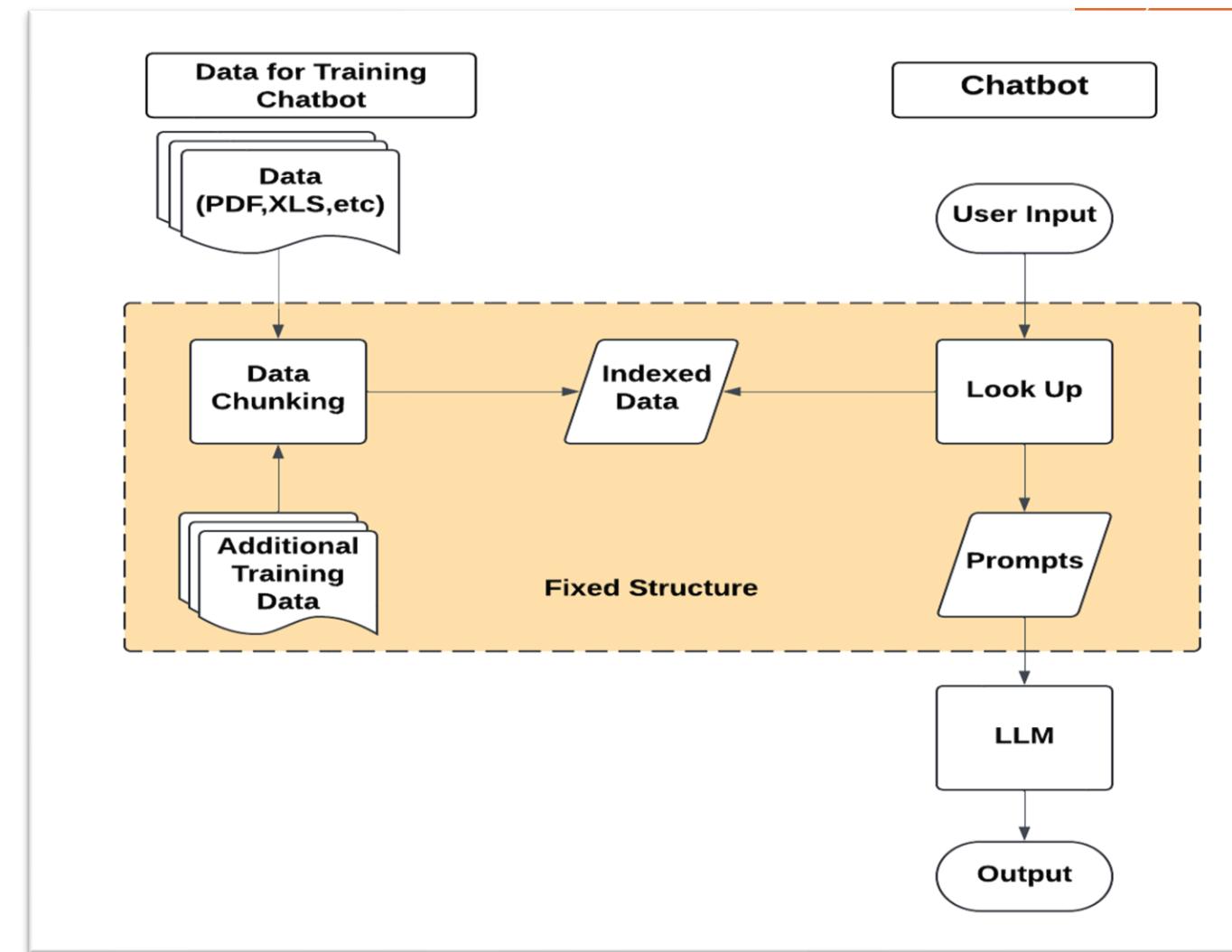
Spec PDF Review

Model  
benchmarking

Prompt and  
response  
recording

Filtering by  
manual  
validation

Excel sheet  
with confidence  
score

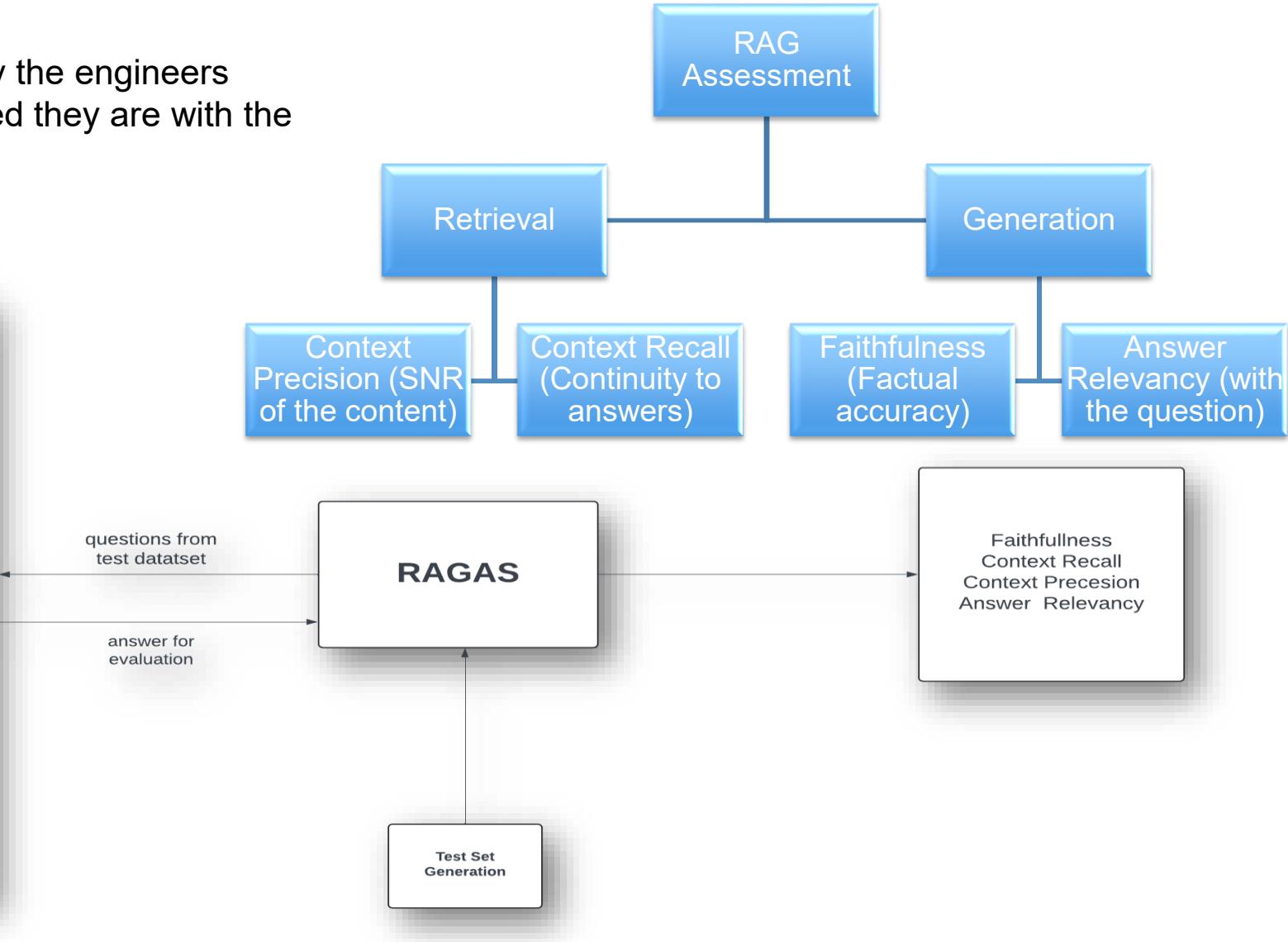
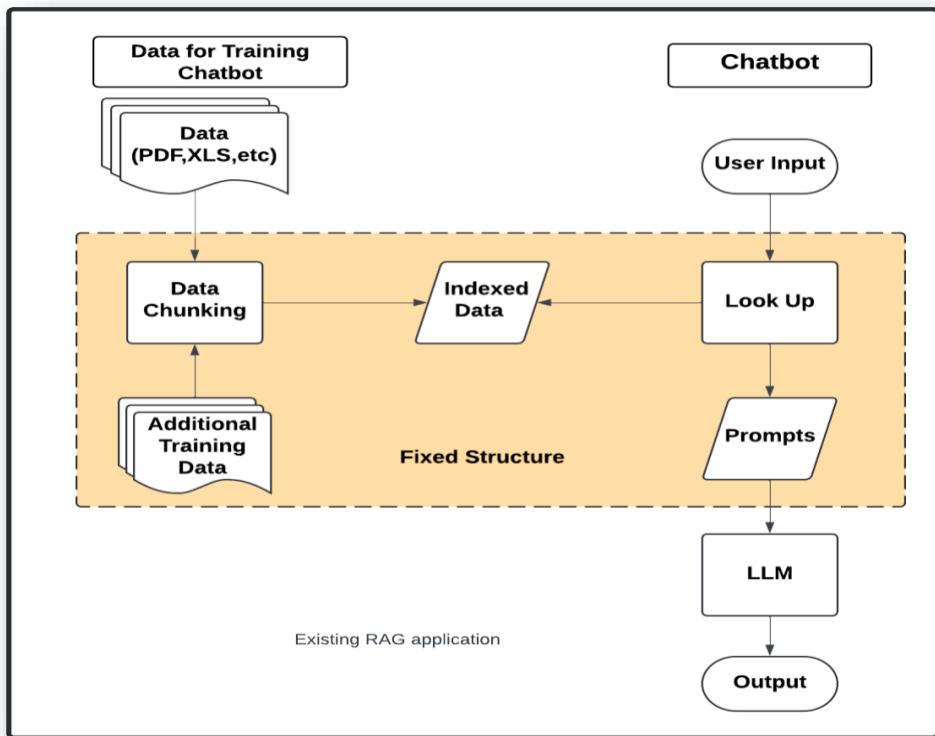


# RAG Assessment

- Manual validation

The generated content is manually validated by the engineers and tagged with *confidence score* (How satisfied they are with the response?)

- RAG Pipeline Assessment



# RAG Assessment

question	answer	contexts	ground_truth	faithfulness	answer_relevancy	context_recall	context_precision
What role do integrated circuits (ICs) play in virtual...	Integrated circuits (ICs) are used in virtual...	[Applications in Electronics]\nThe ability to c...	Integrated circuits (ICs) are fundamental buil...	1.000000	0.946481	1.00	1.0
What are the potential future developments in ...	The future of semiconductors will likely invol...	[Future Directions]\nThe future of semiconducto...	The future of semiconductors is poised for exc...	1.000000	0.992269	1.00	1.0
How does Moore's Law relate to the development...	Moore's Law predicts that the number of transi...	[The Role in Technological Advancement]\nThe co...	Moore's Law predicts that the number of transi...	0.833333	0.936722	1.00	1.0

# **Work with Moore's Lab AI: Reinventing 5 DV Workflows with AI**

Transforming design verification through artificial intelligence

# AI-Powered Verification Workflows

## 1. Testplan Generation

Spec-to-Testplan Automation

## 2. UVM Testbench Creation

Automated UVM Scaffold

## 3. UVM Testcase Implementation

Testplan Items → Sequences

## 4. SVA & Functional Coverage

Assertion Mining & Covergroups Generation

## 5. Debug Automation

Waveform & Log Based Debug Intelligence

# 1. Testplan Generation



01

## Spec-to-Testplan Automation

AI parses natural-language specifications to create structured, coverage-oriented testplans.

02

## Bidirectional Traceability

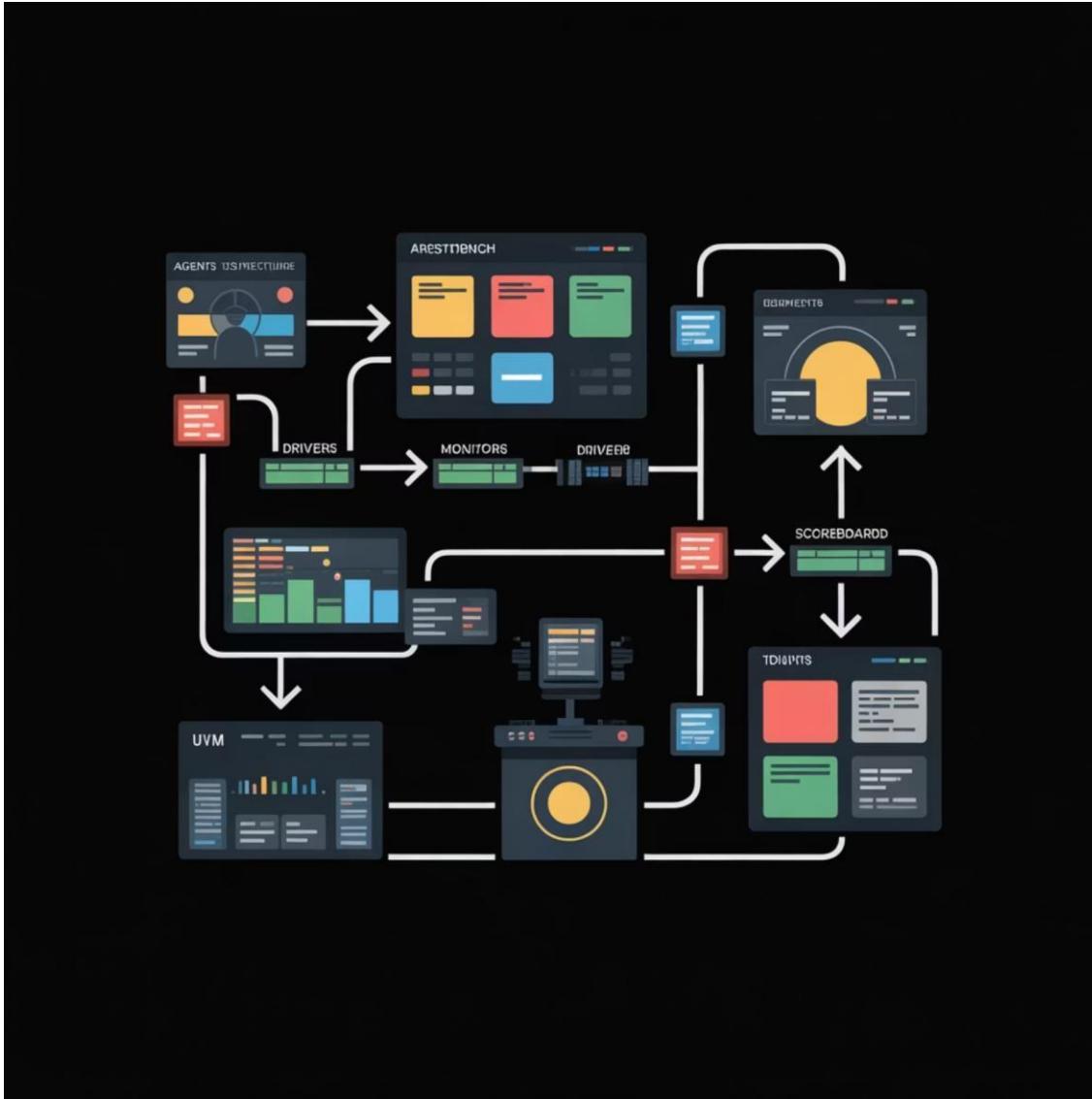
Each test item links directly to spec sections for audit and review by designers and architects.

03

## Dynamic Updates

Auto-sync testplans with evolving specs—incremental regeneration on change detection.

## 2. UVM Testbench Creation



### Automated UVM Scaffold

AI generates UVM agents, drivers, monitors, scoreboards, and connects them per DUT interfaces.

### VIP Reuse Optimization

Recommends internal or third-party VIPs based on past projects and protocol matching.

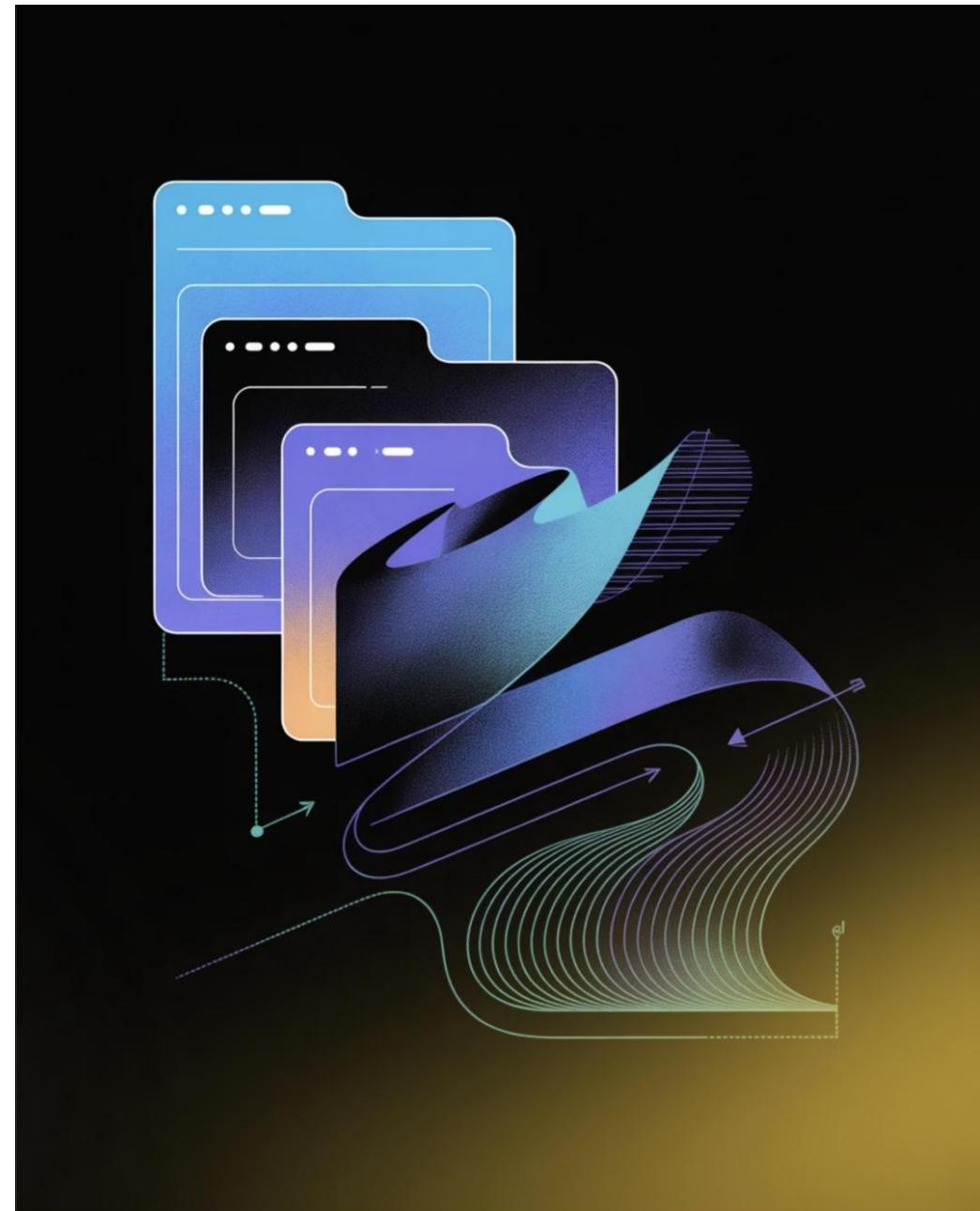
### 3. UVM Testcase Implementation

#### Testplan Items → Sequences

Converts scenario descriptions into runnable UVM sequences with constraints and coverage hooks.

#### Coverage-Driven Refinement

Reinforcement learning generates new stimuli for under-covered covered areas.



# 4. SVA & Functional Coverage

Intelligent property extraction and coverage optimization



## Assertion Mining

Extracts design properties and proposes SystemVerilog Assertions via pattern recognition

## Coverage Groups & Bins

Generate covergroups and coverpoints based on the protocol and architecture specification



# 5. Debug Automation



## Waveform & Log Intelligence

Clusters failures via signal correlation; highlights root-cause candidates.



## Anomaly & Log Summarization

AI summarizes regression logs, flags behavioral outliers, and identifies failure trends.



# Summary

- Infrastructure and security
- Deployment for Design Verification at Tessolve
- Automating generation for UVM test benches, tests, coverage and debug
  - Using Moore's Lab AI

# Thank You!

## CONTACT US TODAY:

Mike Bartley, Founder/CEO, Alpinum Consulting

[mike@alpinumconsulting.com](mailto:mike@alpinumconsulting.com)

+44 (0) 7796 307958

Visit our website



Book a call



LinkedIn

