Encarsia:
Evaluating CPU Fuzzers via Automatic Bug Injection

Matej Bölcskei, Flavien Solt, Katharina Ceesay-Seitz, and Kaveh Razavi

How do hardware fuzzers work?

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They are automated test benches

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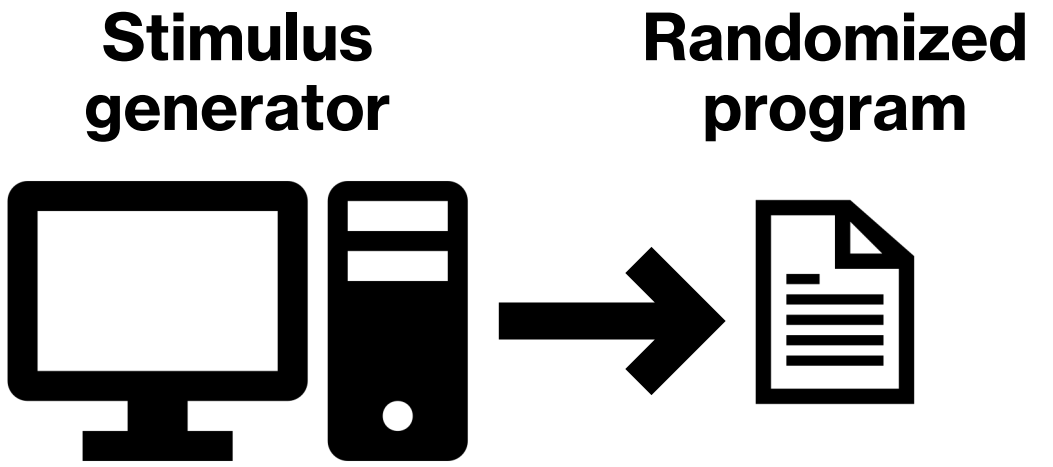

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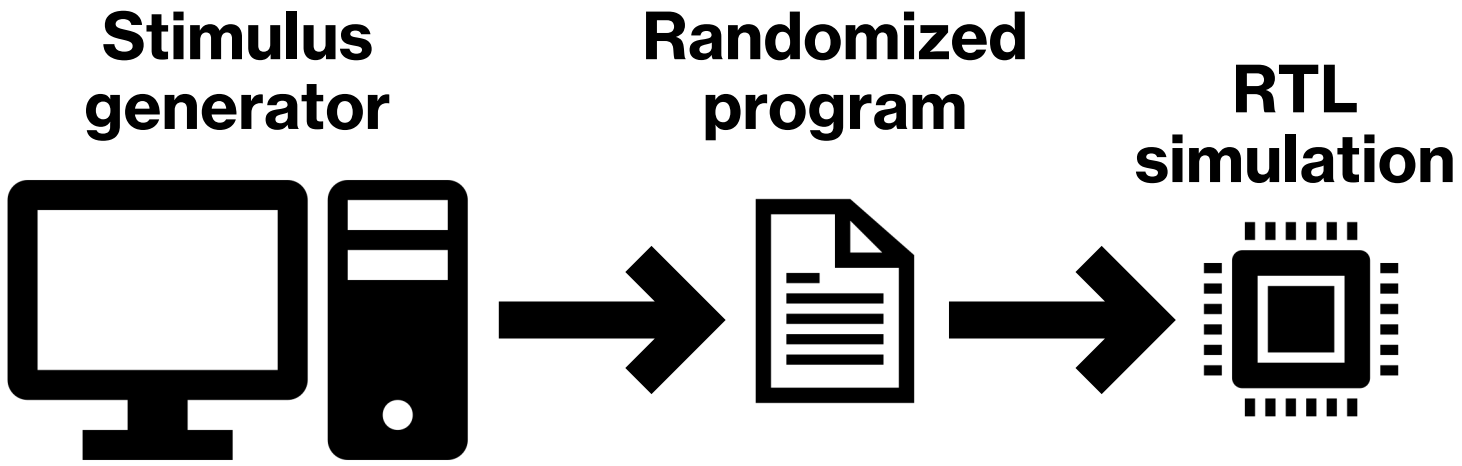

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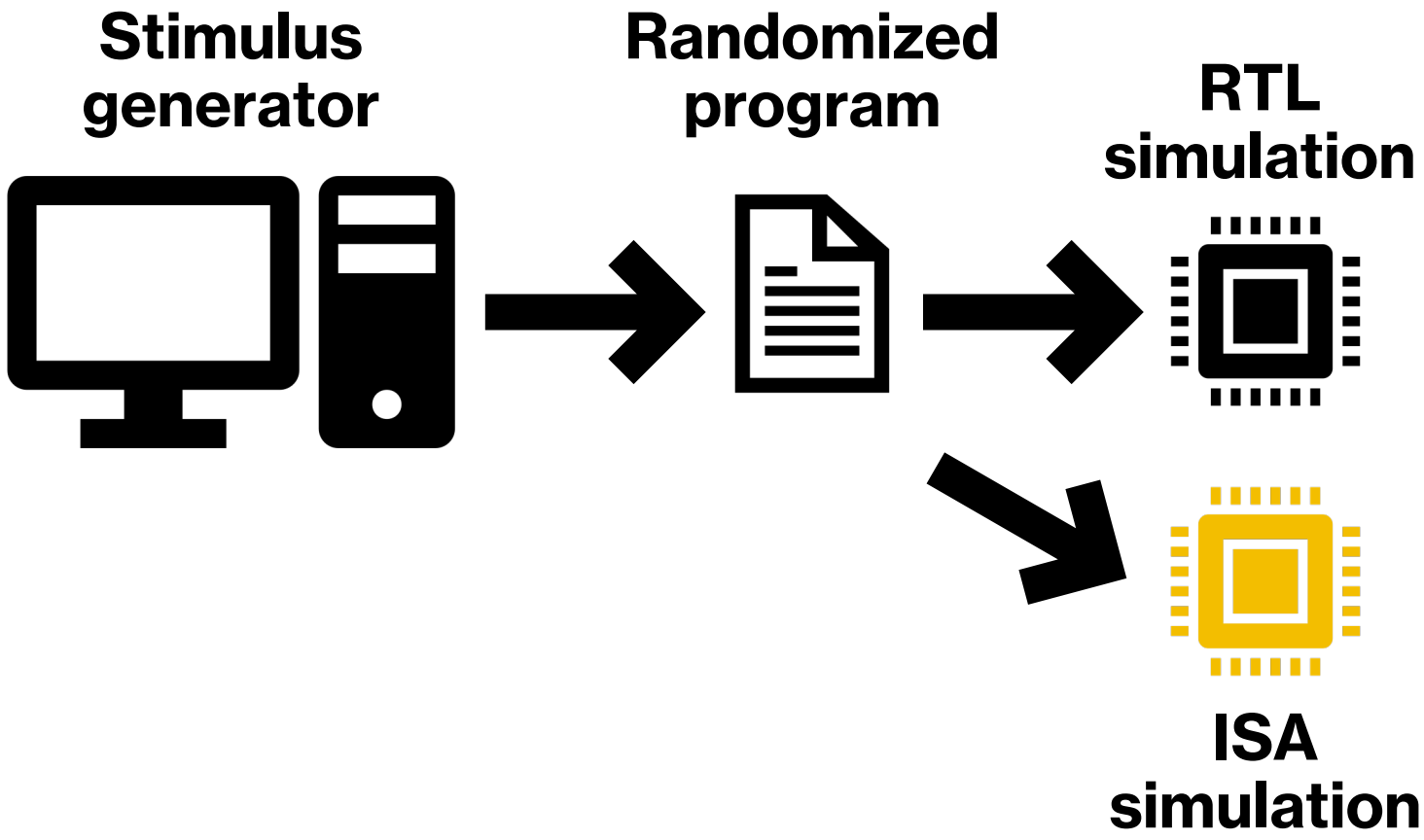

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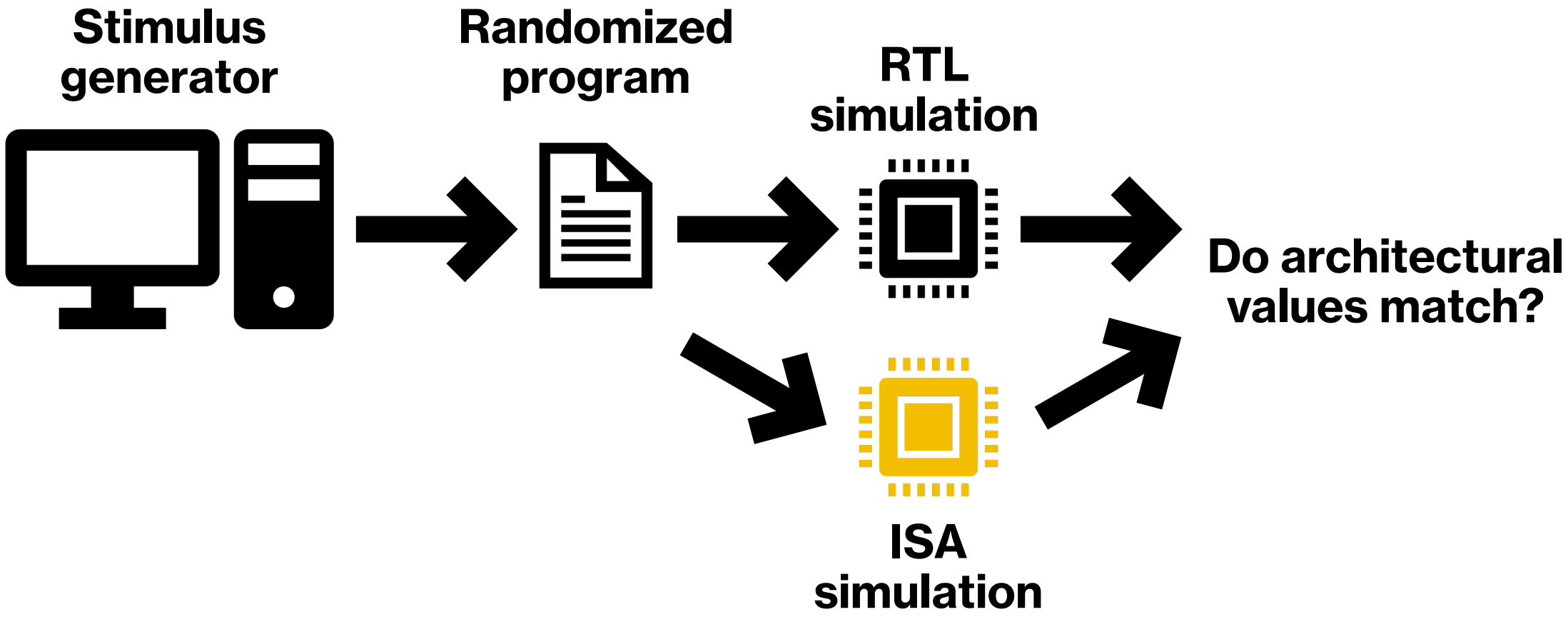

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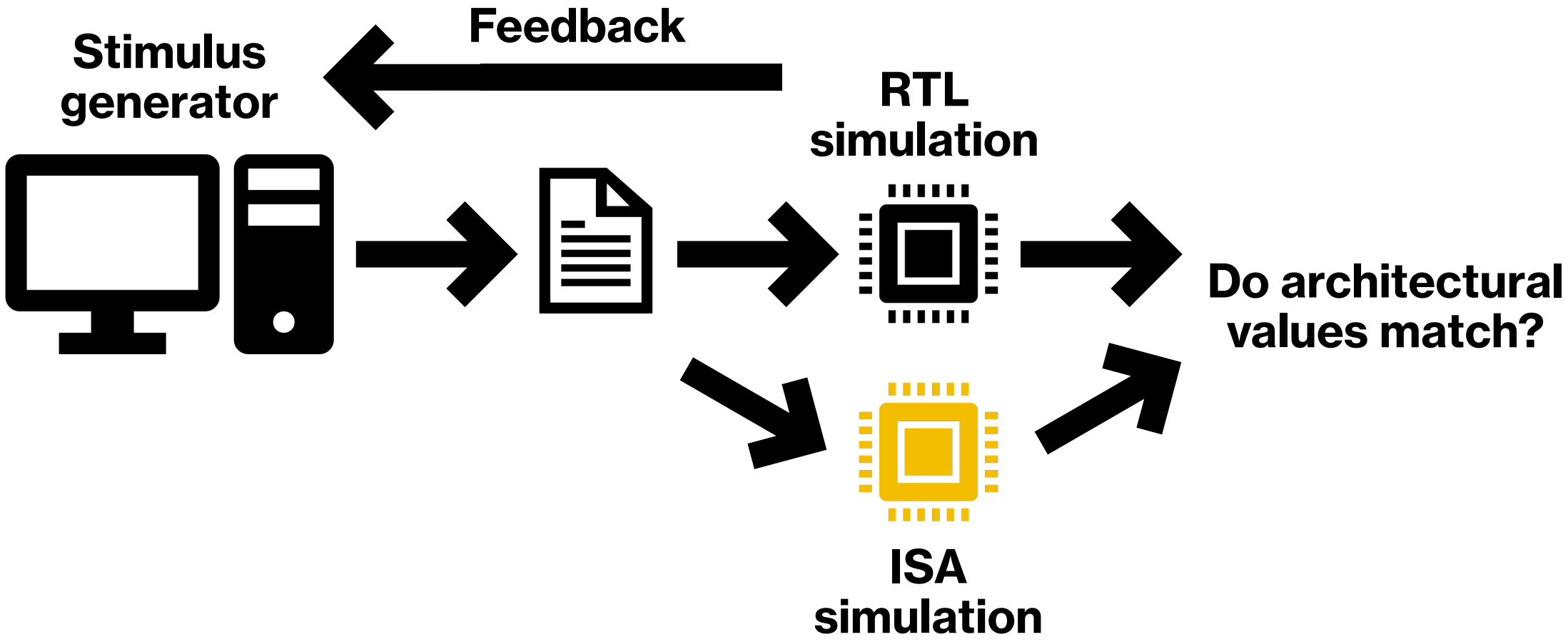

Fuzzers look great on paper

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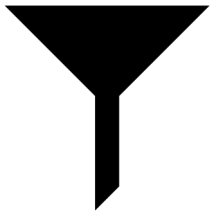
They achieve high coverage!



Multiplexer

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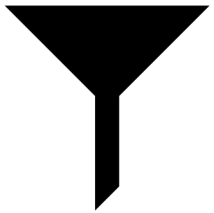

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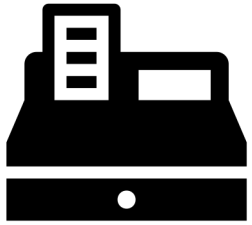

Register

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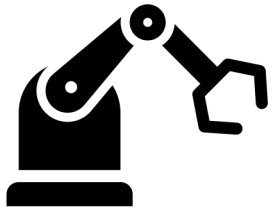
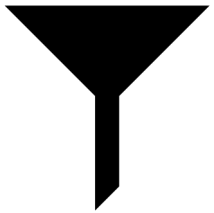


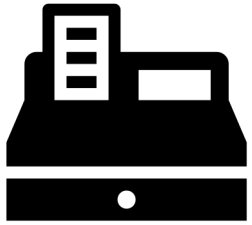
FSM



Multiplexer

Edge

Branch



Register

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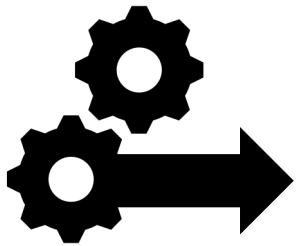

Output

Statement

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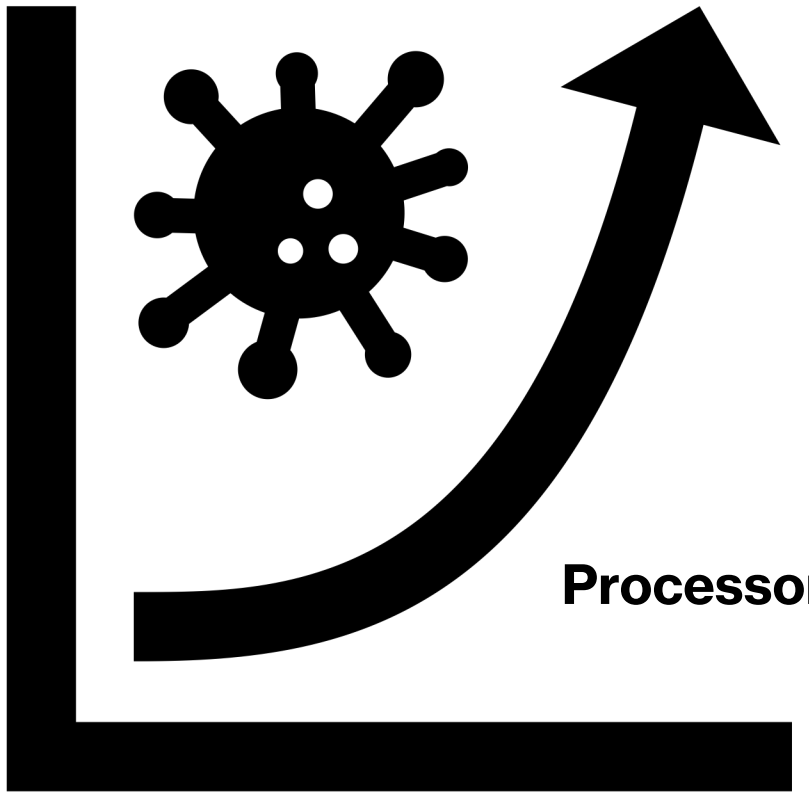

ProcessorFuzz: 9 bugs

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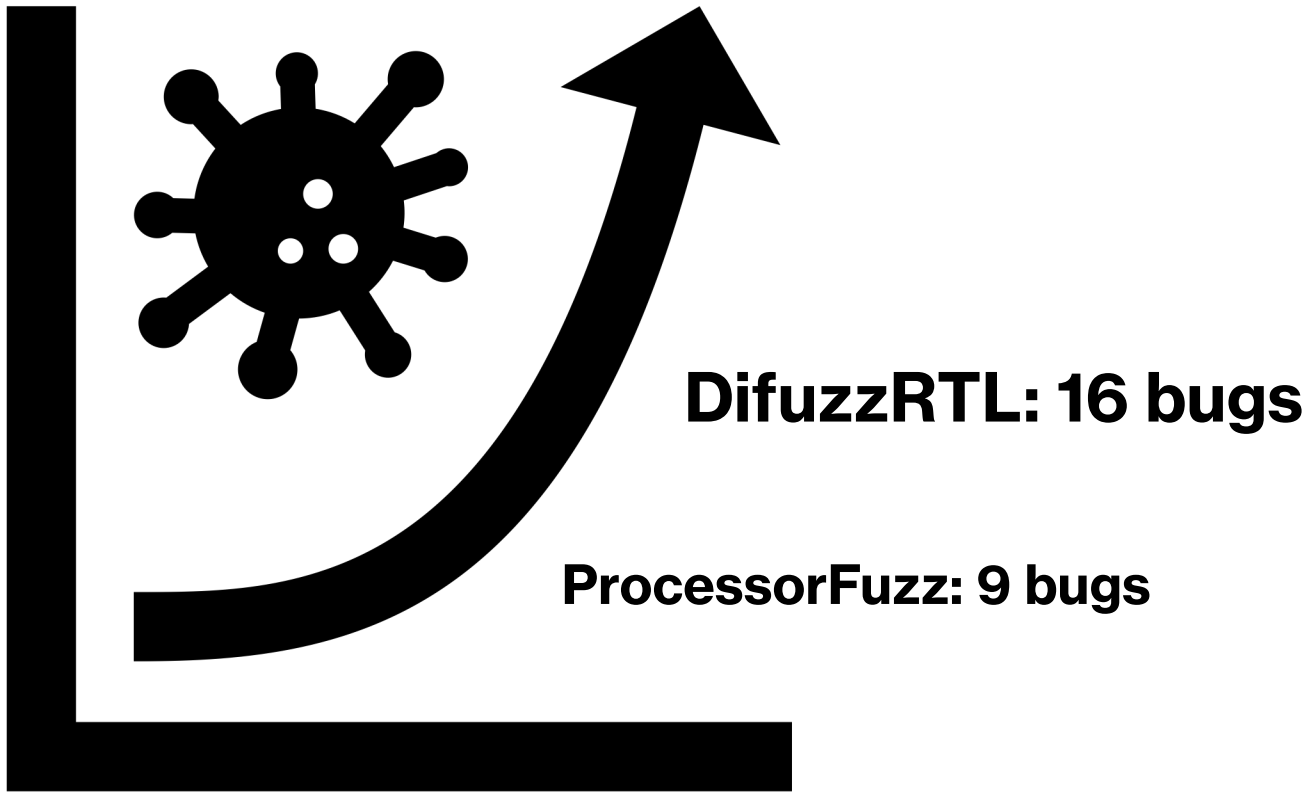

DifuzzRTL: 16 bugs

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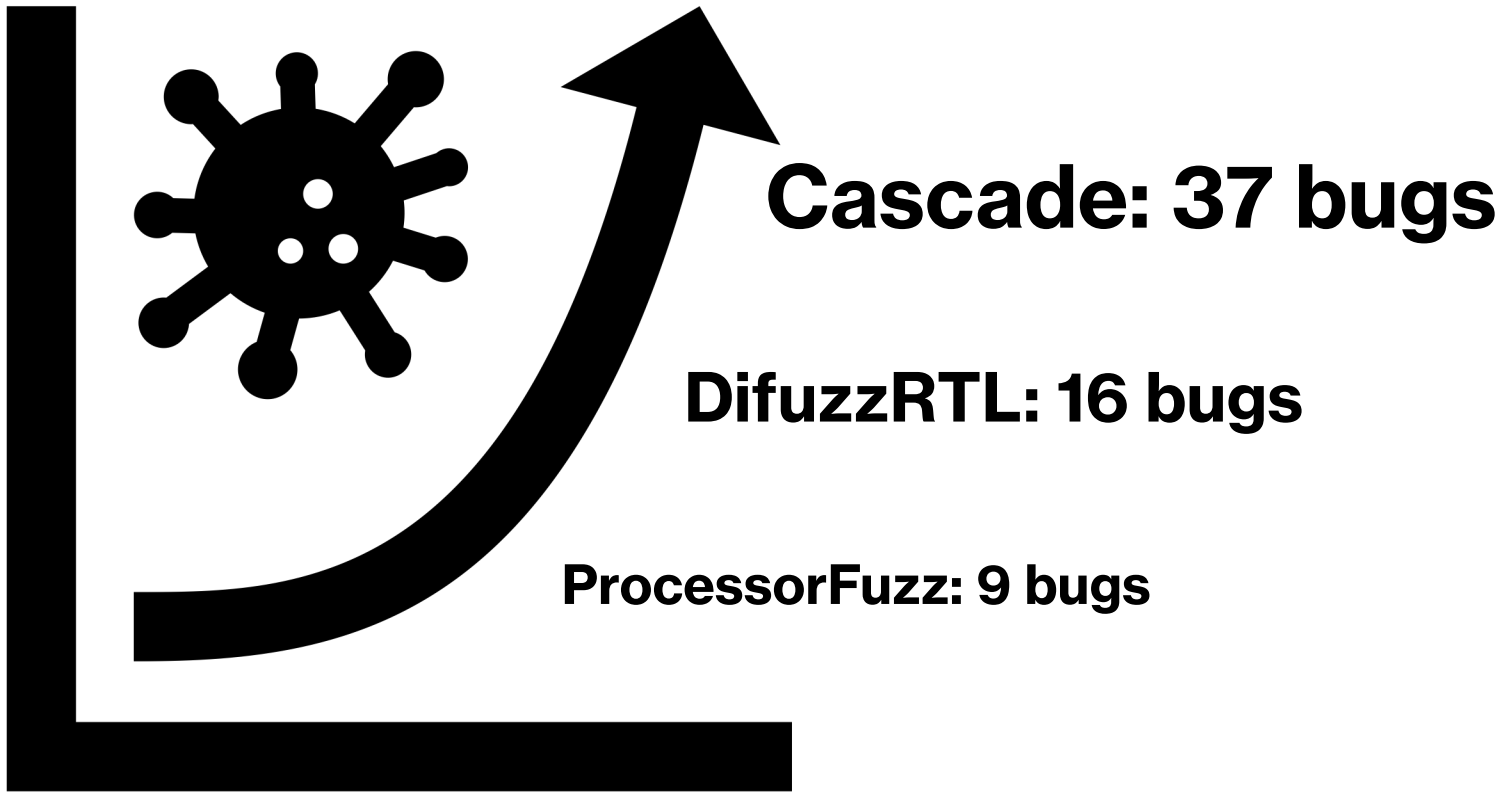

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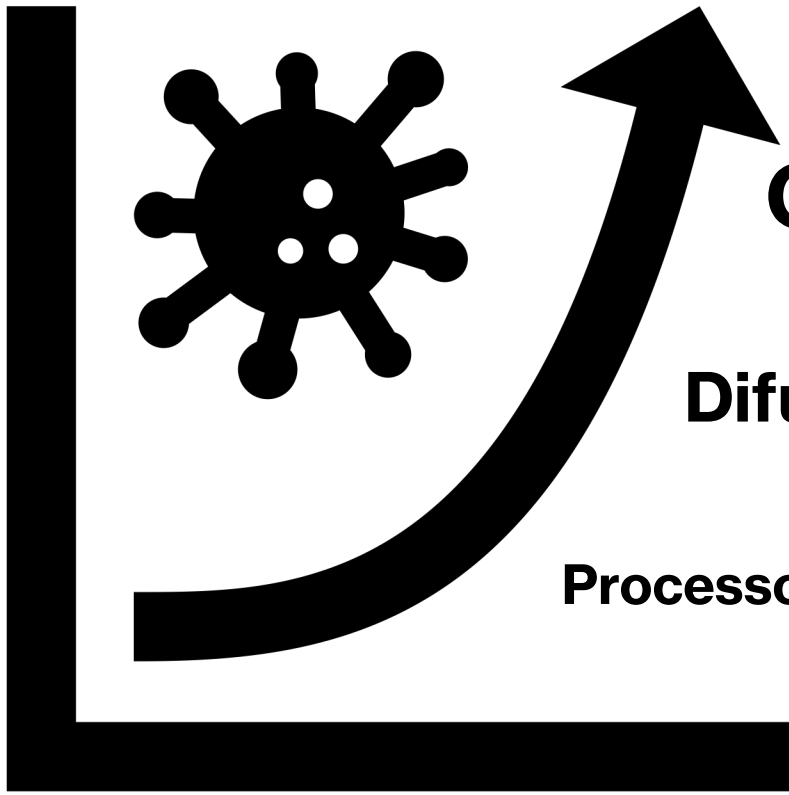

Everybody gets a bug!

Cascade: 37 bugs

DifuzzRTL: 16 bugs

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Creators use flashy figures to sell stories

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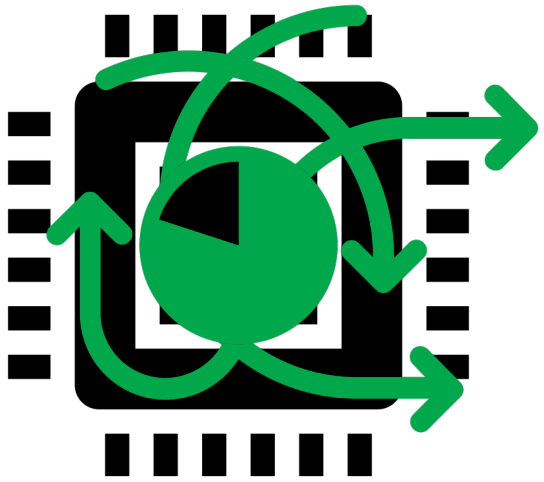
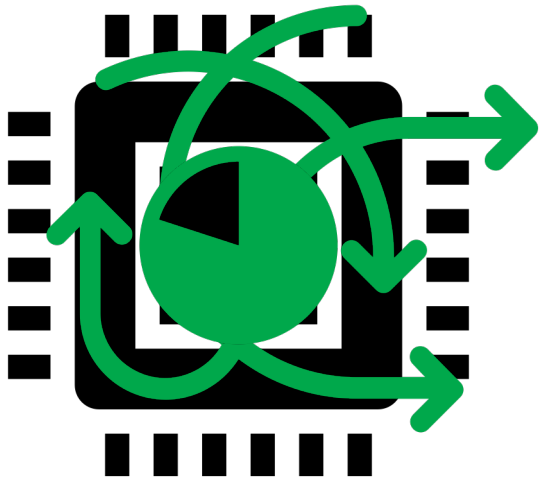


Design coverage

Creators use flashy figures to sell stories



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Bug detection

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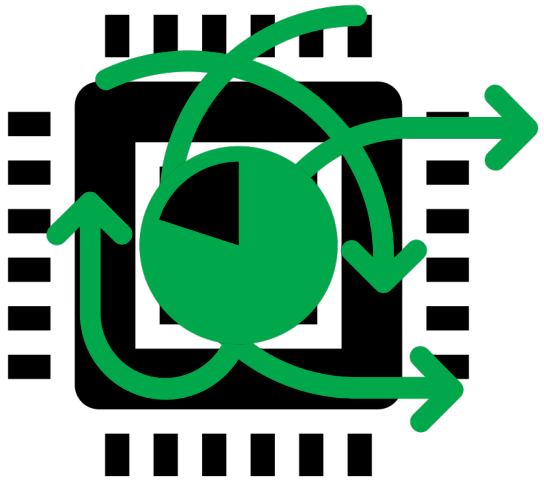

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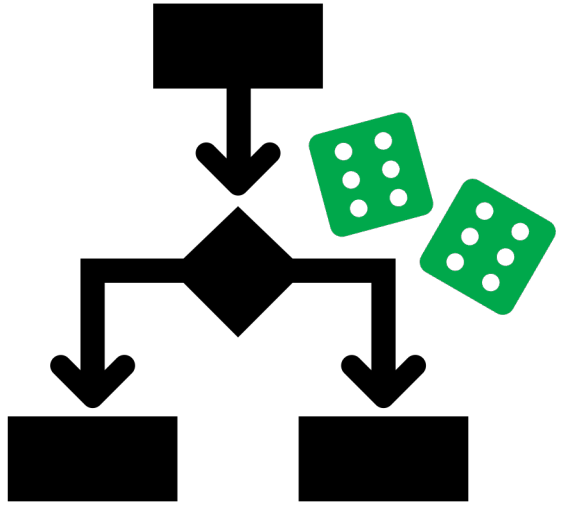

Input generation

Fuzzer evaluation is flawed

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Coverage is not well suited for comparing fuzzers

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“Coverage is not strongly correlated with test suite ...”
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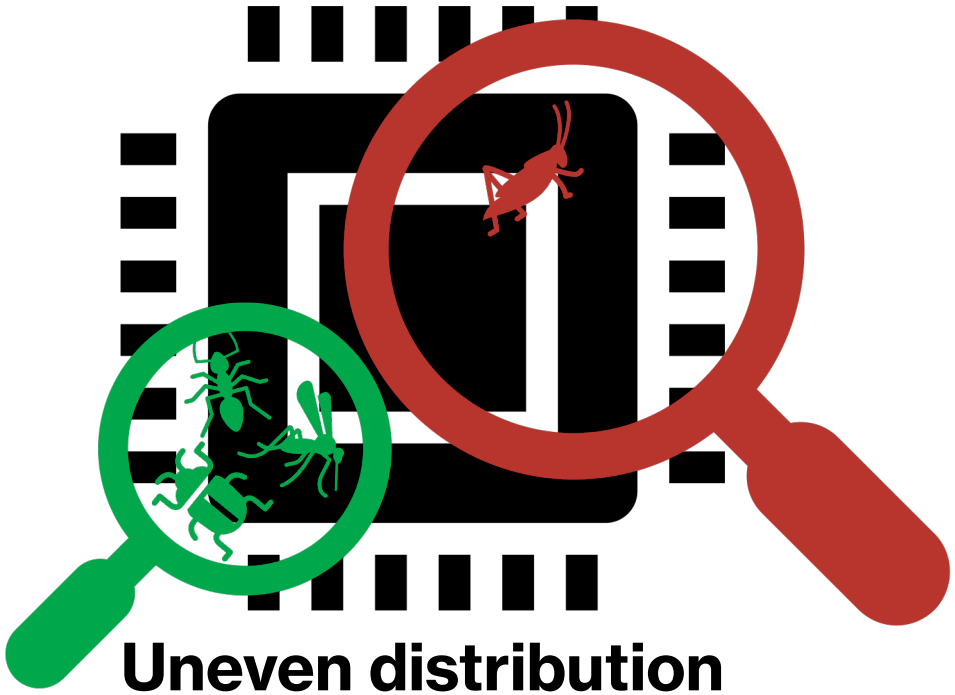

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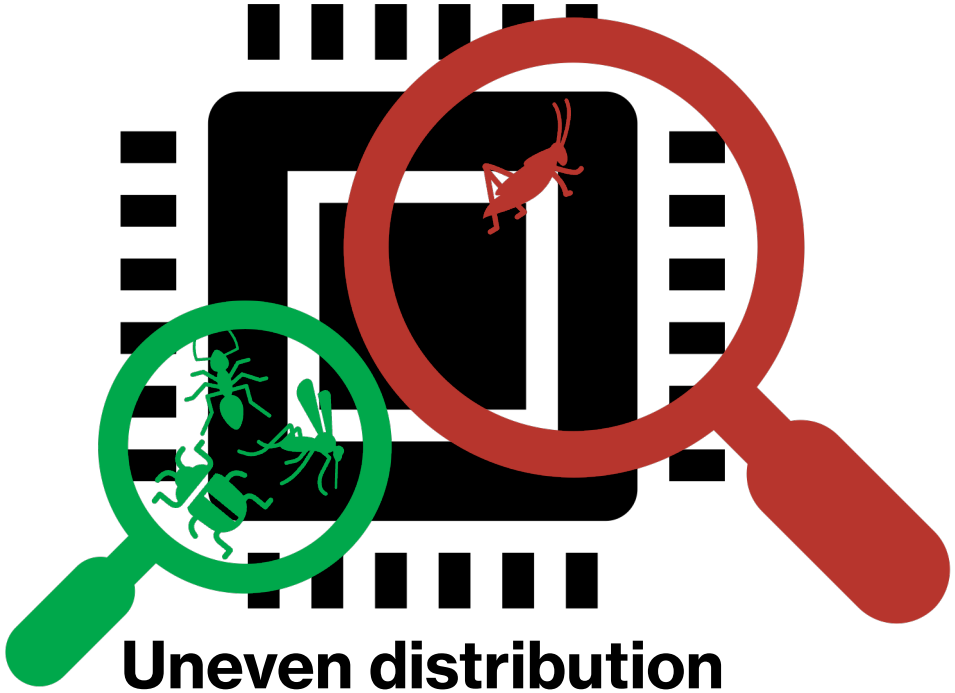

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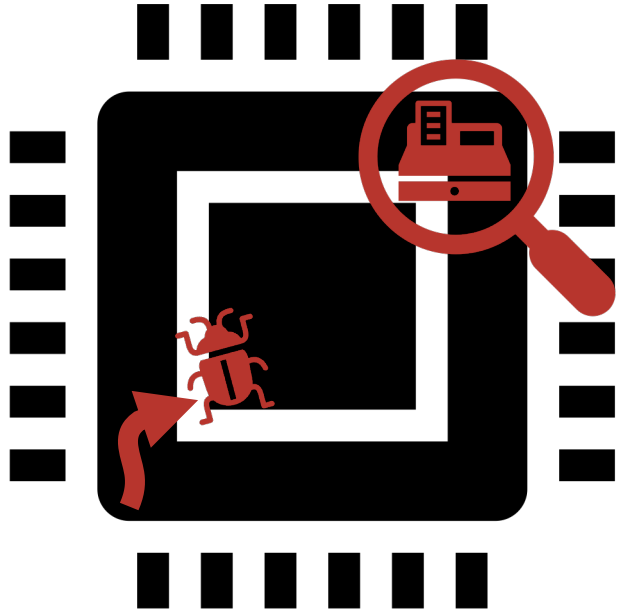

Ignores propagation

Fuzzer evaluation is flawed

Let’s examine bug discovery

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Let’s examine bug discovery

Bug	Device	Description
1	BlackParrot	Non-boxed single-precision floating point ...
2	BlackParrot	Read-after-Write dependencies on fcsr.fflags ...
3	BlackParrot	When mstatus.FS is not set and the fcsr is ...
4	BlackParrot	The 2 low-bits of sepc CSR are not ...
5	BlackParrot	No exception raised when writing certain ..
6	BlackParrot	Reading zero register, following specific ...
7	Dromajo	PMP checks are performed, and raise ...
8	Rocket & BOOM	Instruction page fault not raised when ...
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Never Fuzzed

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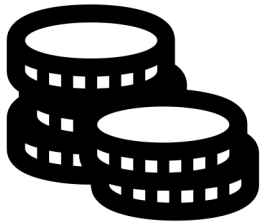

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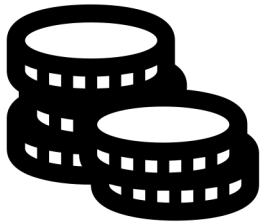

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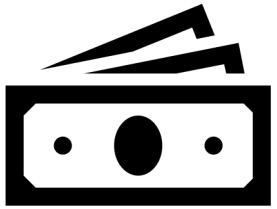

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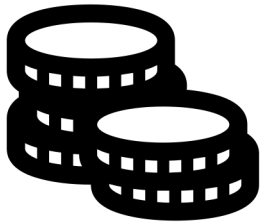

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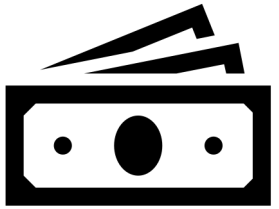

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Contradiction!

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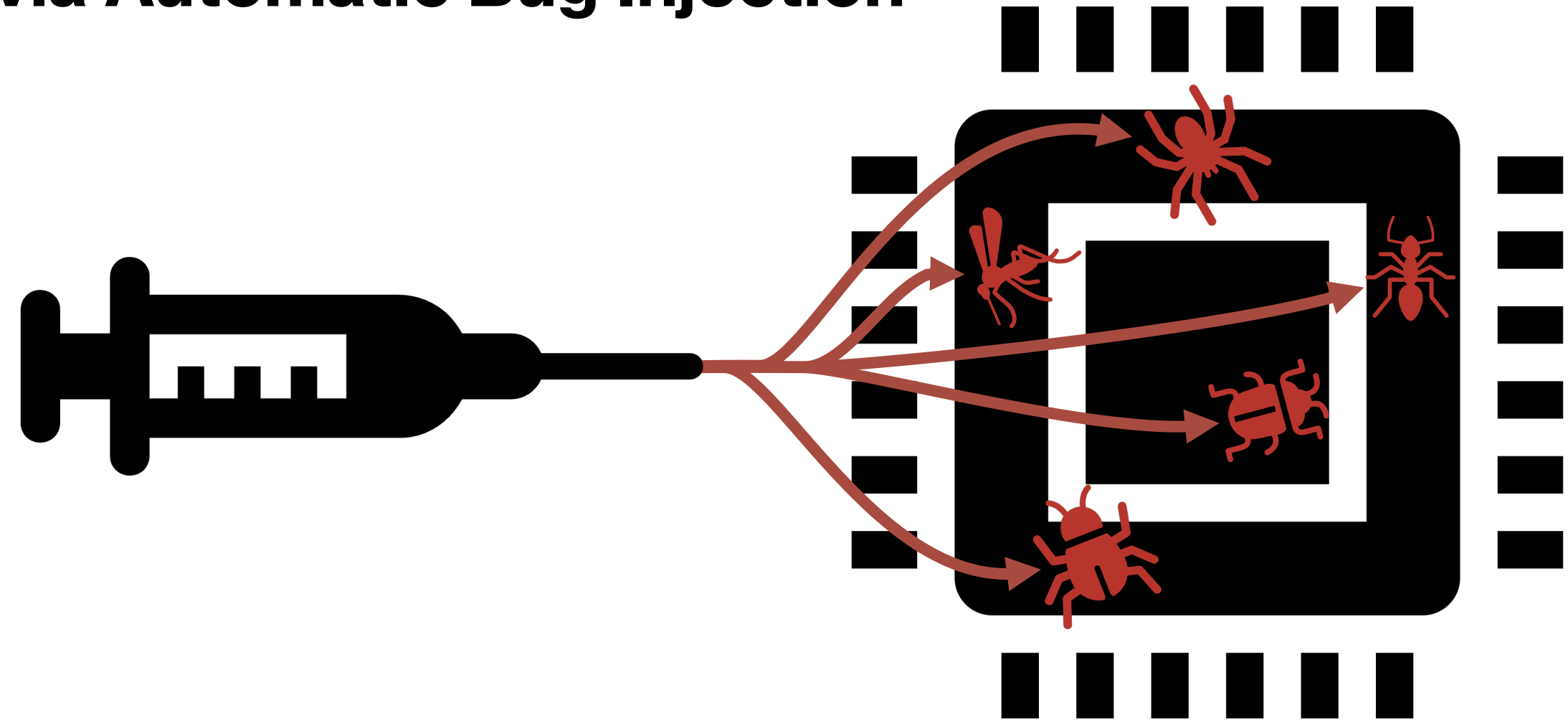

How do bugs arise in the real world?

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We survey 1672 pull requests

#399 Prevents illegal CSR writes

Accessing a debug register outside of debug mode sets illegal_csr, but the CSR write still happened. This change ensures that if an illegal CSR instruction is signaled, the CSR write is blocked.

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assign illegal_csr_insn_o =
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```

Source	Conditionals	Mix-ups	Other
Ibex	17	14	0
CVA6	22	11	0
Rocket	8	41	0
BOOM	13	33	0
DAC19	2	2	0
DAC21	4	10	0
Total	66	111	0

All 177 bugs fall into 2 categories

How do bugs arise in the real world?

Signal Mix-ups

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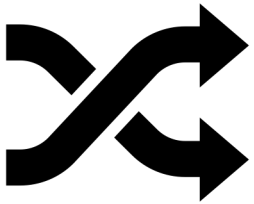
Definition



Confusing similar signals

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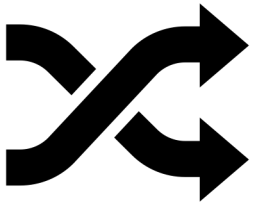

Confusing similar signals

Broken Conditionals

```
illegal_csr   = 1'b0;
case (csr_addr_i)
    CSR_MSTATUS: csr_rdata_int = mstatus_q
    CSR_DCSR: begin
        csr_rdata_int = dcsr_q;
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    end
    default: illegal_csr = 1'b1;
endcase
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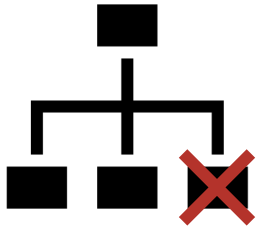

Mishandling corner cases

How do we inject bugs?

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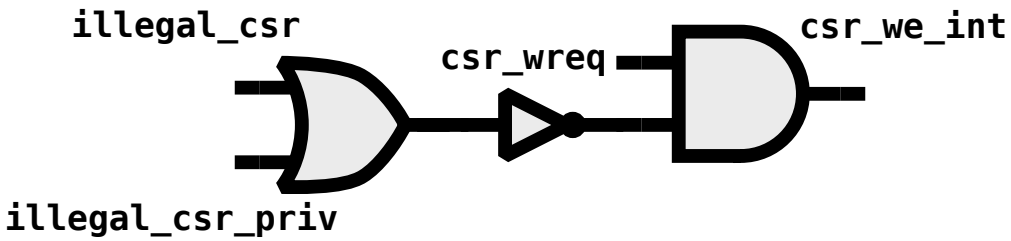
Intermediate representation



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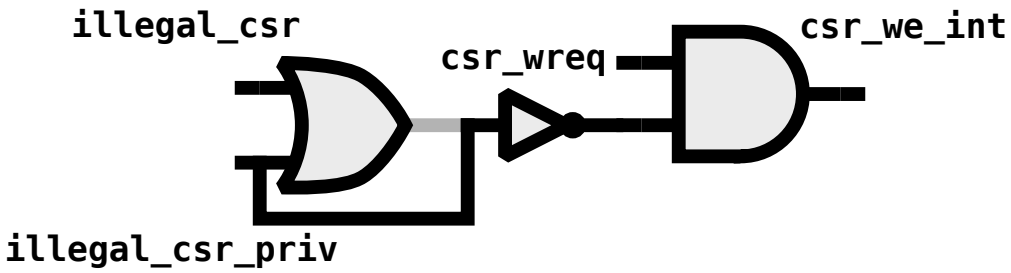

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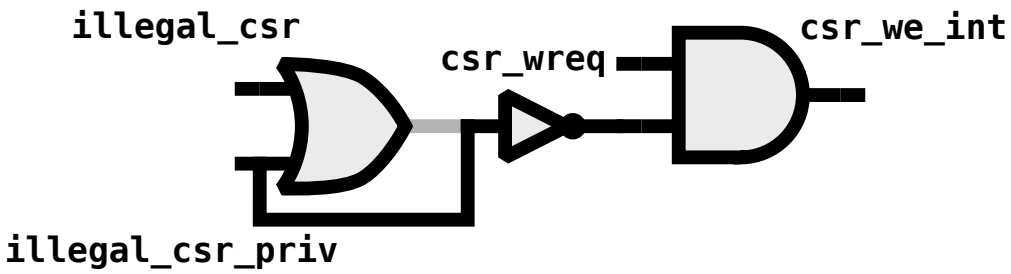

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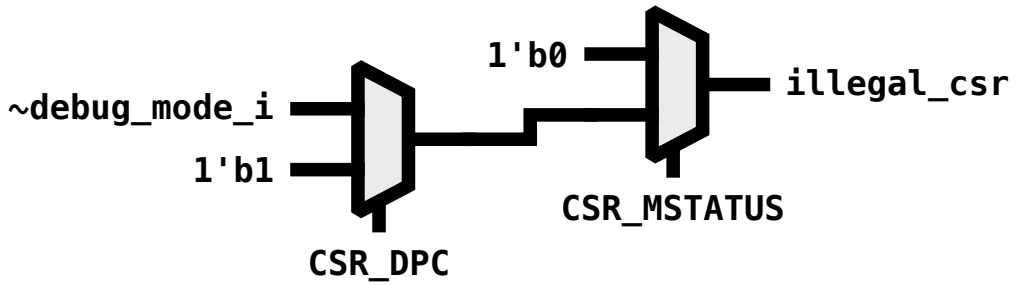

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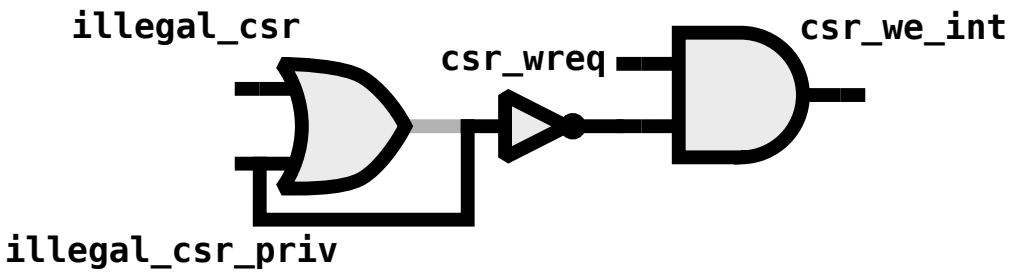

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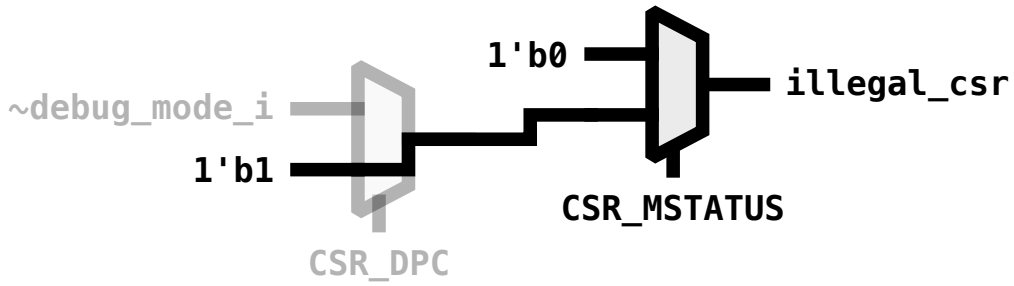

What about ineffective transformations?

We formally verify architectural observability

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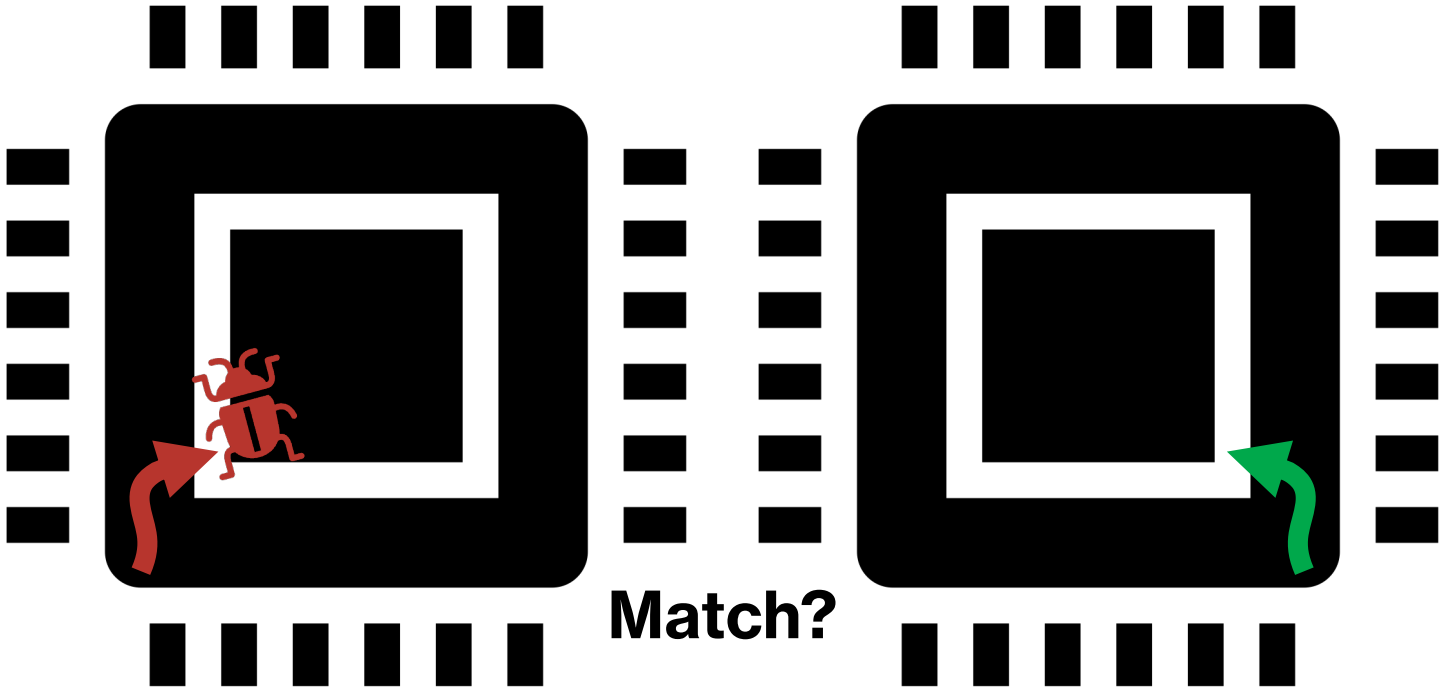
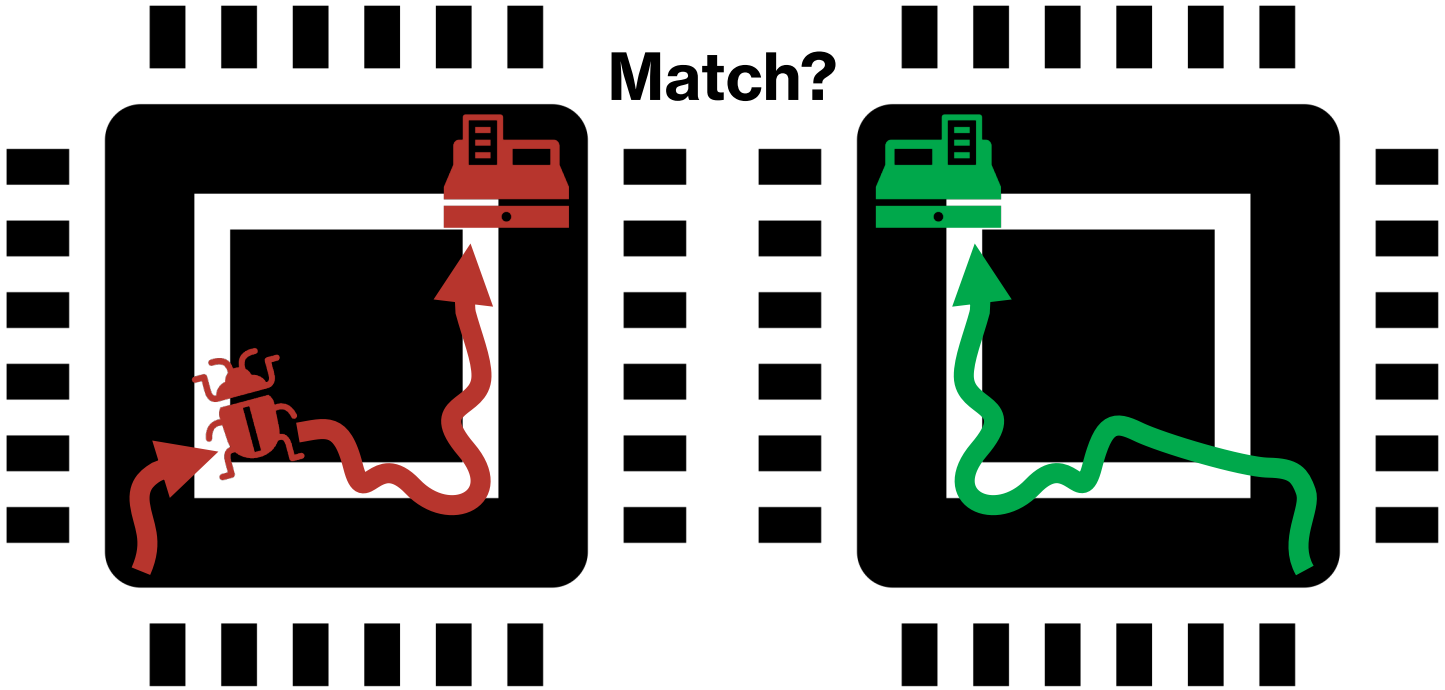
We formally verify architectural observability



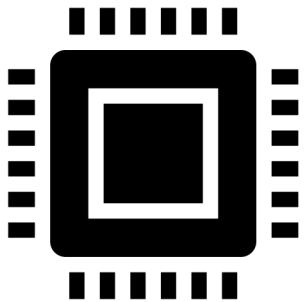
What about ineffective transformations?

We formally verify architectural observability

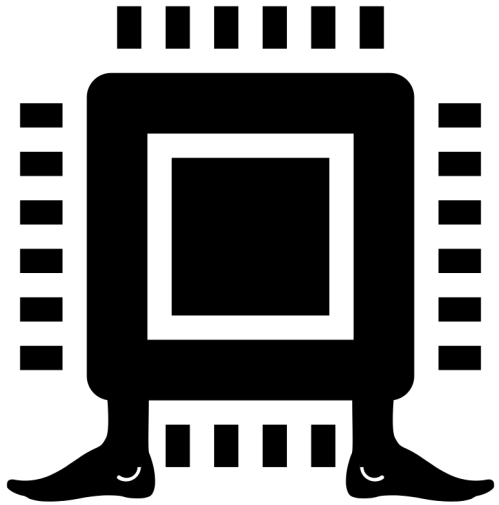


Which fuzzing techniques actually work?

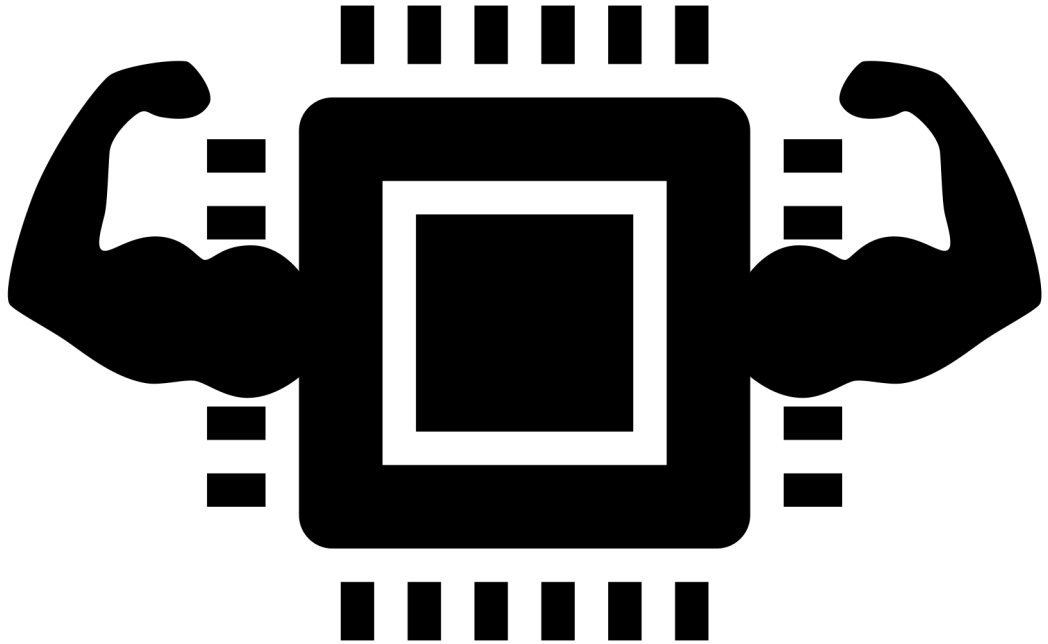
We generate EnCorpus



Ibex



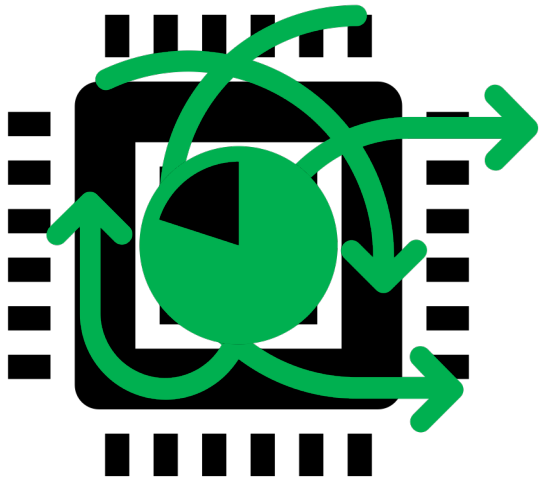
Rocket



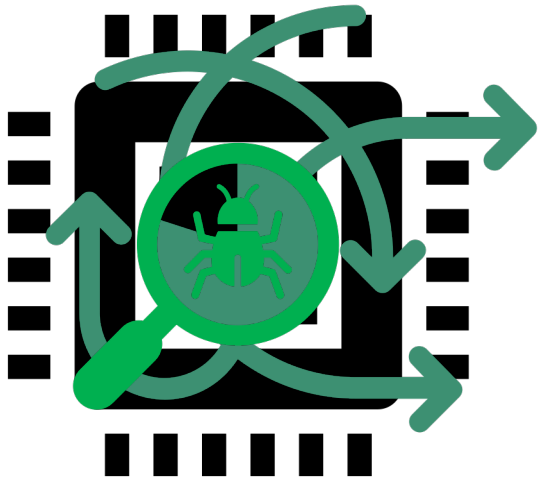
BOOM

Which fuzzing techniques actually work?

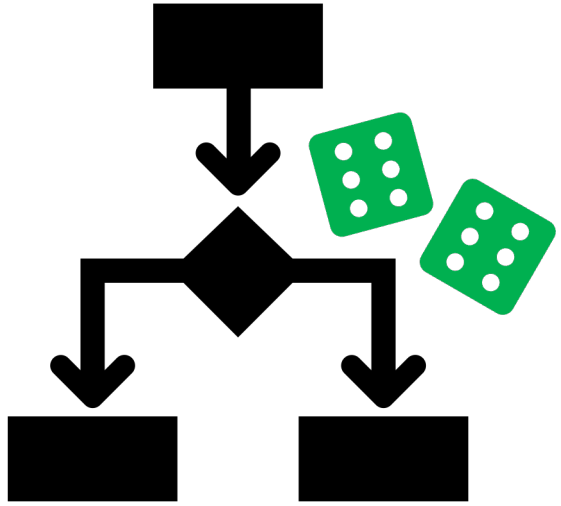
We must test each technique in isolation



DifuzzRTL

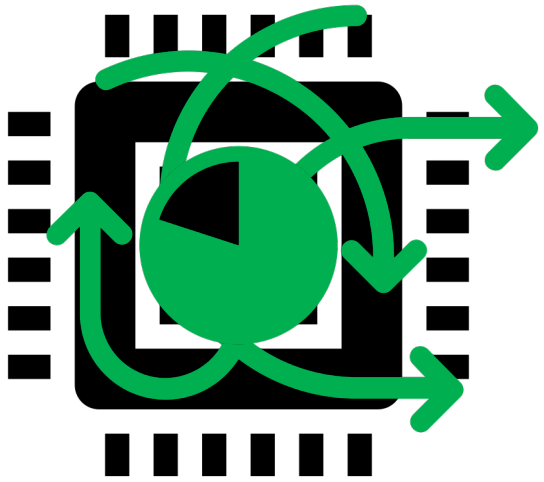


ProcessorFuzz

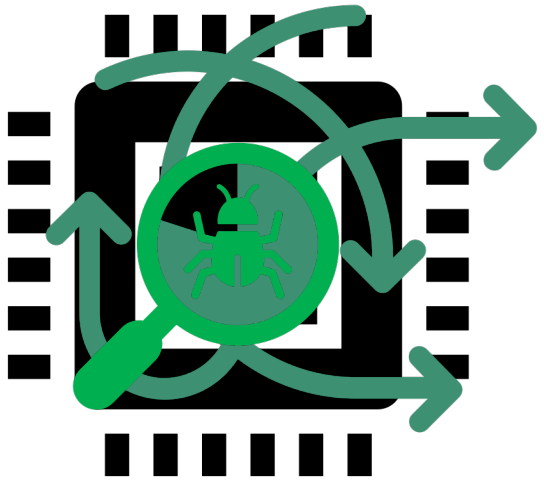


Cascade

Is instruction-granular detection worth it?

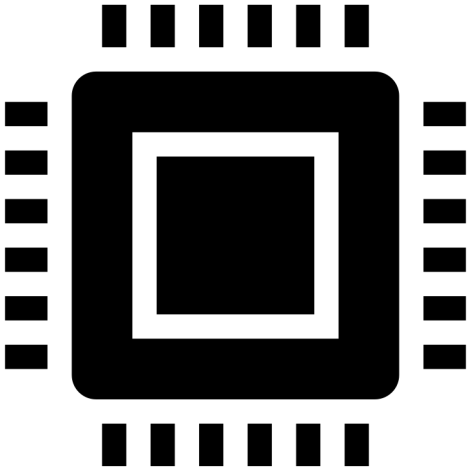


DifuzzRTL



ProcessorFuzz

Is instruction-granular detection worth it?



DifuzzRTL

ProcessorFuzz

Is instruction-granular detection worth it?

Rocket

Signal Mix-ups

Fuzzer	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
DifRTL	✗	✓	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✓	✗	✓
PFuzz	✗	✓	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✓	✗	✓

Broken Conditionals

Fuzzer	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
DifRTL	✗	✗	✗	✗	✗	✓	✓	✗	✗	✓	✗	✓	✗	✗	✓
PFuzz	✗	✗	✗	✗	✗	✓	✓	✗	✗	✓	✗	✓	✗	✗	✓

BOOM

Signal Mix-ups

Fuzzer	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
DifRTL	✓	✓	✗	✓	✓	✗	✗	✓	✗	✓	✓	✓	✗	✗	✓
PFuzz	✓	✓	✗	✓	✓	✗	✗	✓	✗	✓	✓	✓	✗	✗	✓

Broken Conditionals

Fuzzer	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
DifRTL	✓	✓	✗	✗	✗	✗	✓	✗	✗	✗	✓	✓	✗	✗	✓
PFuzz	✓	✓	✗	✗	✗	✗	✓	✗	✗	✗	✓	✓	✗	✗	✓

Is instruction-granular detection worth it?

Rocket

Signal Mix-ups

Fuzzer	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
DifRTL	✗	✓	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✓	✗	✓
PFuzz	✗	✓	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✓	✗	✓

Broken Conditionals

Fuzzer	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
DifRTL	✗	✗	✗	✗	✗	✓	✓	✗	✗	✓	✗	✓	✗	✗	✓
PFuzz	✗	✗	✗	✗	✗	✓	✓	✗	✗	✓	✗	✓	✗	✗	✓

BOOM

Signal Mix-ups

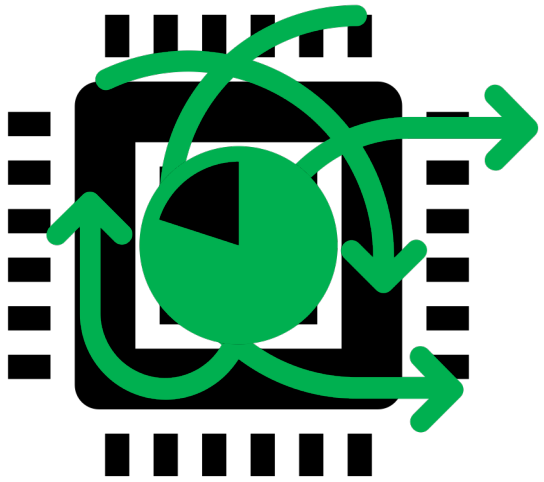
Fuzzer	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
DifRTL	✓	✓	✗	✓	✓	✗	✗	✓	✗	✓	✓	✓	✗	✗	✓
PFuzz	✓	✓	✗	✓	✓	✗	✗	✓	✗	✓	✓	✓	✗	✗	✓

Broken Conditionals

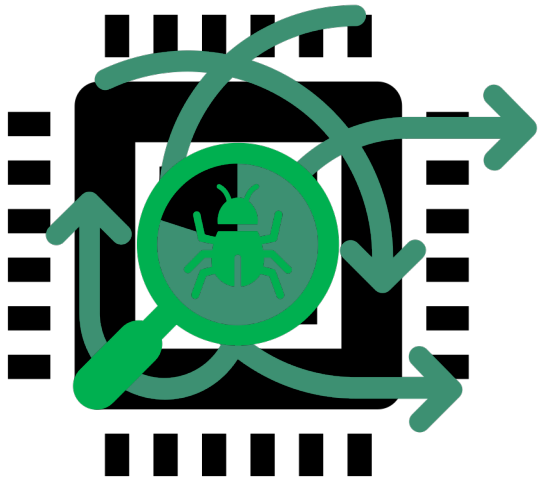
Fuzzer	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
DifRTL	✓	✓	✗	✗	✗	✗	✓	✗	✗	✗	✓	✓	✗	✗	✓
PFuzz	✓	✓	✗	✗	✗	✗	✓	✗	✗	✗	✓	✓	✗	✗	✓

Insight 1:
Finer detection granularity does not yield better results.

Are hardware coverage metrics effective?



DifuzzRTL



ProcessorFuzz

Are hardware coverage metrics effective?

Rocket

Signal Mix-ups

Cover.	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
None	✗	✓	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✓	✗	✓
DifRTL	✗	✓	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✓	✗	✓
PFuzz	✗	✓	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✓	✗	✓

Broken Conditionals

Cover.	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
None	✗	✗	✗	✗	✗	✓	✓	✗	✗	✓	✗	✓	✗	✗	✓
DifRTL	✗	✗	✗	✗	✗	✓	✓	✗	✗	✓	✗	✓	✗	✗	✓
PFuzz	✗	✗	✗	✗	✗	✓	✓	✗	✗	✓	✗	✓	✗	✗	✓

BOOM

Signal Mix-ups

Cover.	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
None	✓	✓	✗	✓	✓	✗	✗	✓	✗	✓	✓	✓	✗	✗	✓
DifRTL	✓	✓	✗	✓	✓	✗	✗	✓	✗	✓	✓	✓	✗	✗	✓
PFuzz	✓	✓	✗	✓	✓	✗	✗	✓	✗	✓	✓	✓	✗	✗	✓

Broken Conditionals

Cover.	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
None	✓	✓	✗	✗	✗	✗	✓	✗	✗	✗	✓	✓	✗	✗	✓
DifRTL	✓	✓	✗	✗	✗	✗	✓	✗	✗	✗	✓	✓	✗	✗	✓
PFuzz	✓	✓	✗	✗	✗	✗	✓	✗	✗	✗	✓	✓	✗	✗	✓

Are hardware coverage metrics effective?

Rocket

Signal Mix-ups

Cover.	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
None	✗	✓	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✓	✗	✓
DifRTL	✗	✓	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✓	✗	✓
PFuzz	✗	✓	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✓	✗	✓

Broken Conditionals

Cover.	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
None	✗	✗	✗	✗	✗	✓	✓	✗	✗	✓	✗	✓	✗	✗	✓
DifRTL	✗	✗	✗	✗	✗	✓	✓	✗	✗	✓	✗	✓	✗	✗	✓
PFuzz	✗	✗	✗	✗	✗	✓	✓	✗	✗	✓	✗	✓	✗	✗	✓

BOOM

Signal Mix-ups

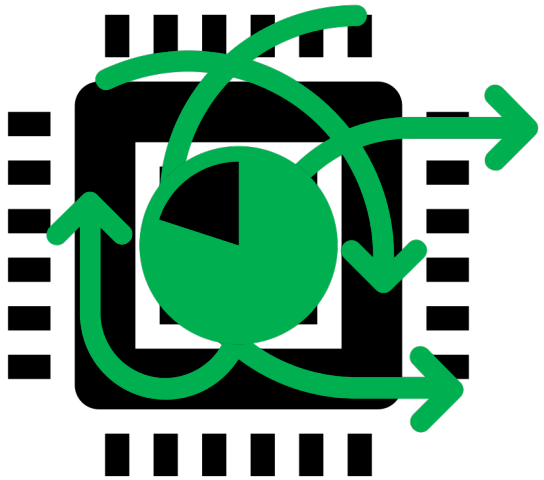
Cover.	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
None	✓	✓	✗	✓	✓	✗	✗	✓	✗	✓	✓	✓	✗	✗	✓
DifRTL	✓	✓	✗	✓	✓	✗	✗	✓	✗	✓	✓	✓	✗	✗	✓
PFuzz	✓	✓	✗	✓	✓	✗	✗	✓	✗	✓	✓	✓	✗	✗	✓

Broken Conditionals

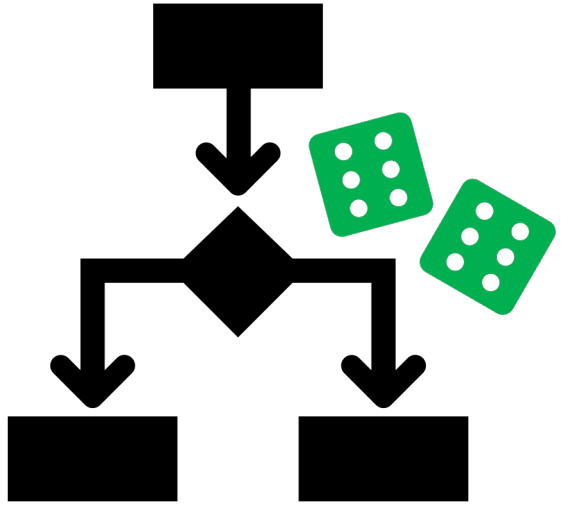
Cover.	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
None	✓	✓	✗	✗	✗	✗	✓	✗	✗	✗	✓	✓	✗	✗	✓
DifRTL	✓	✓	✗	✗	✗	✗	✓	✗	✗	✗	✓	✓	✗	✗	✓
PFuzz	✓	✓	✗	✗	✗	✗	✓	✗	✗	✗	✓	✓	✗	✗	✓

Insight 2:
Coverage metrics do not effectively guide fuzzers.

Does program generation play a role?



DifuzzRTL



Cascade

Does program generation play a role?

Rocket

Signal Mix-ups

Fuzzer	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
DifRTL	✗	✓	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✓	✗	✓
Cascade	✓	✓	✓	✓	✗	✓	✗	✗	✗	✗	✗	✗	✓	✗	✓

Broken Conditionals

Fuzzer	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
DifRTL	✗	✗	✗	✗	✗	✓	✓	✗	✗	✓	✗	✓	✗	✗	✓
Cascade	✗	✓	✗	✗	✗	✓	✗	✗	✗	✗	✗	✓	✗	✗	✓

BOOM

Signal Mix-ups

Fuzzer	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
DifRTL	✓	✓	✗	✓	✓	✗	✗	✓	✗	✓	✓	✓	✗	✗	✓
Cascade	✓	✓	✗	✗	✗	✓	✓	✓	✓	✓	✓	✗	✗	✓	✓

Broken Conditionals

Fuzzer	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
DifRTL	✓	✓	✗	✗	✗	✗	✓	✗	✗	✗	✓	✓	✗	✗	✓
Cascade	✓	✓	✗	✗	✗	✗	✓	✗	✗	✗	✓	✓	✗	✗	✗

Does program generation play a role?

Rocket

Signal Mix-ups

Fuzzer	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
DifRTL	✗	✓	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✓	✗	✓
Cascade	✓	✓	✓	✓	✗	✓	✗	✗	✗	✗	✗	✗	✓	✗	✓

Broken Conditionals

Fuzzer	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
DifRTL	✗	✗	✗	✗	✗	✓	✓	✗	✗	✓	✗	✓	✗	✗	✓
Cascade	✗	✓	✗	✗	✗	✓	✗	✗	✗	✗	✗	✓	✗	✗	✓

BOOM

Signal Mix-ups

Fuzzer	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
DifRTL	✓	✓	✗	✓	✓	✗	✗	✓	✗	✓	✓	✓	✗	✗	✓
Cascade	✓	✓	✗	✗	✗	✓	✓	✓	✓	✓	✓	✗	✗	✓	✓

Broken Conditionals

Fuzzer	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
DifRTL	✓	✓	✗	✗	✗	✗	✓	✗	✗	✗	✓	✓	✗	✗	✓
Cascade	✓	✓	✗	✗	✗	✗	✓	✗	✗	✗	✓	✓	✗	✗	✗

Insight 3:
Program generation is the primary driver of finding bugs.

Encarsia helps detect misconfigurations

DifuzzRTL

Bug	Detected	Module
5	✓	UOPCodeFDivDec ...
6	✗	DivUnit
7	✗	MulDiv
8	✓	IntToFP
9	✗	PipelinedMulUnit
10	✓	ALU
11	✓	RegisterReadDecode

Encarsia helps detect misconfigurations

DifuzzRTL

Bug	Detected	Module
5	✓	UOPCodeFDivDec ...
6	✗	DivUnit
7	✗	MulDiv
8	✓	IntToFP
9	✗	PipelinedMulUnit
10	✓	ALU
11	✓	RegisterReadDecode

Forgets the M extension

```
def __init__(self, isa='RV64G'):
    isas = []
    if 'I' in isa:
        isas += [ 'rv32i' ]
    if 'M' in isa:
        isas += [ 'rv32m' ]
    if 'A' in isa:
        isas += [ 'rv32a' ]
    if 'F' in isa:
        isas += [ 'rv32f' ]
    if 'G' in isa:
--      isas = ['rv32i', 'rv32m', 'rv32a', 'rv32f']
```

Encarsia helps detect misconfigurations

DifuzzRTL

Bug	Detected	Module
5	✓	UOPCodeFDivDec ...
6	✗	DivUnit
7	✗	MulDiv
8	✓	IntToFP
9	✗	PipelinedMulUnit
10	✓	ALU
11	✓	RegisterReadDecode

Forgets the M extension

```
def __init__(self, isa='RV64G'):
    isas = []
    if 'I' in isa:
        isas += [ 'rv32i' ]
    if 'M' in isa:
        isas += [ 'rv32m' ]
    if 'A' in isa:
        isas += [ 'rv32a' ]
    if 'F' in isa:
        isas += [ 'rv32f' ]
    if 'G' in isa:
--      isas = ['rv32i', 'rv32m', 'rv32a', 'rv32f']
```

Insight 4:
Fuzzers do not test the entire ISA

Encarsia helps detect flaws

Cascade

Bug	Detected	Module
1	✓	IssueSlot
2	✓	Arbiter_16
3	✗	DivSqrtRecF64_mul ...
4	✗	DivSqrtRecF64_mul ...
5	✗	UOPCodeFDivDec ...
6	✓	DivUnit
7	✓	MulDiv
8		IntToFP
⋮	⋮	

Encarsia helps detect flaws

Cascade

Bug	Detected	Module
1	✓	IssueSlot
2	✓	Arbiter_16
3	✗	DivSqrtRecF64_mul ...
4	✗	DivSqrtRecF64_mul ...
5	✗	UOPCodeFDivDec ...
6	✓	DivUnit
7	✓	MulDiv
8		IntToFP
⋮		

Excludes whole instructions

```
if cpu == "cva6":
    probability["fsqrt.d"] = 0

    if not tolerate_cva6_division():
        probability["fdiv.d"] = 0

    if not tolerate_cva6_single_precision():
        probability["fsqrt.s"] = 0
        probability["fdiv.s"] = 0

if cpu == "boom":
++  probability["fsqrt.d"] = 0
++  probability["fdiv.d"] = 0
```

Encarsia helps detect flaws

Cascade

Bug	Detected	Module
1	✓	IssueSlot
2	✓	Arbiter_16
3	✗	DivSqrtRecF64_mul ...
4	✗	DivSqrtRecF64_mul ...
5	✗	UOPCodeFDivDec ...
6	✓	DivUnit
7	✓	MulDiv
8		IntToFP
⋮		⋮

Excludes whole instructions

```
if cpu == "cva6":
    probability["fsqrt.d"] = 0

    if not tolerate_cva6_division():
        probability["fdiv.d"] = 0

    if not tolerate_cva6_single_precision():
        probability["fsqrt.s"] = 0
        probability["fdiv.s"] = 0

if cpu == "boom":
++  probability["fsqrt.d"] = 0
++  probability["fdiv.d"] = 0
```

Insight 5:
Filtering mechanisms hinder the discovery of further bugs

Encarsia injects complex bugs

Encarsia injects complex bugs

BOOM Broken Conditional #3

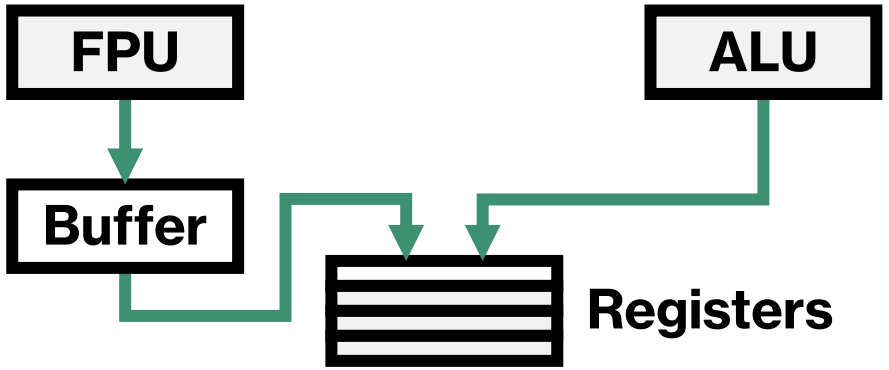
```
if (reset) begin
    enq_ptr <= 3'h0;
end else if (do_enq) begin
    if (wrap) begin
        enq_ptr <= 3’h0;
++  end
end else begin
        enq_ptr <= enq_ptr + 1;
--  end
end
```

Encarsia injects complex bugs

BOOM Broken Conditional #3

```
if (reset) begin
    enq_ptr <= 3'h0;
end else if (do_enq) begin
    if (wrap) begin
        enq_ptr <= 3'h0;
++  end
end else begin
        enq_ptr <= enq_ptr + 1;
--  end
end
```

Buffer between FPU and GRs



Encarsia injects complex bugs

BOOM Broken Conditional #3

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if (reset) begin
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end else if (do_enq) begin
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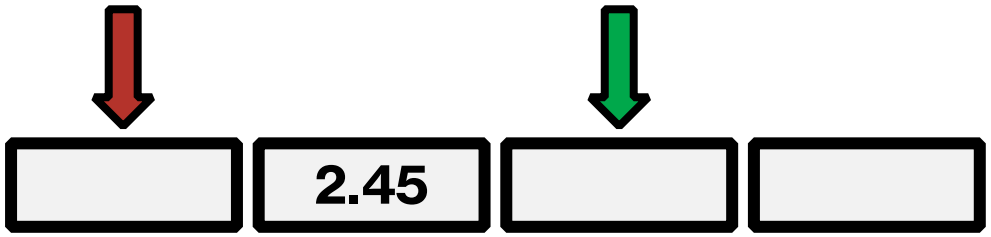
++  end
end else begin
        enq_ptr <= enq_ptr + 1;
--  end
end
```



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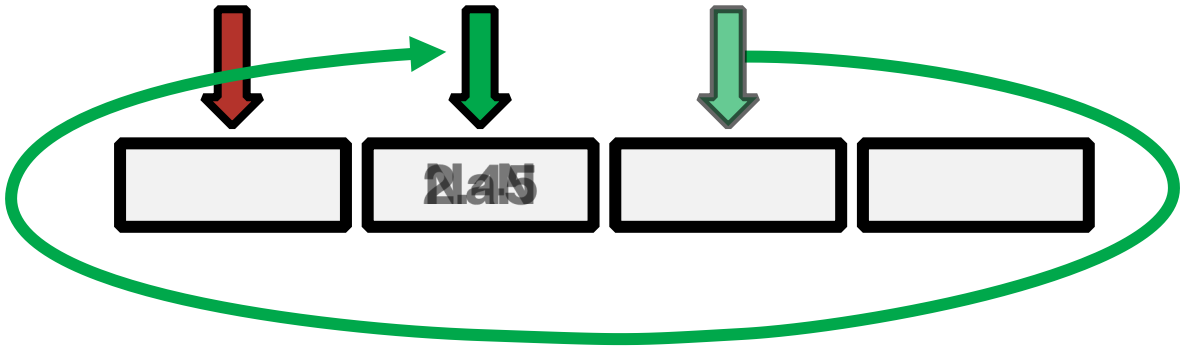

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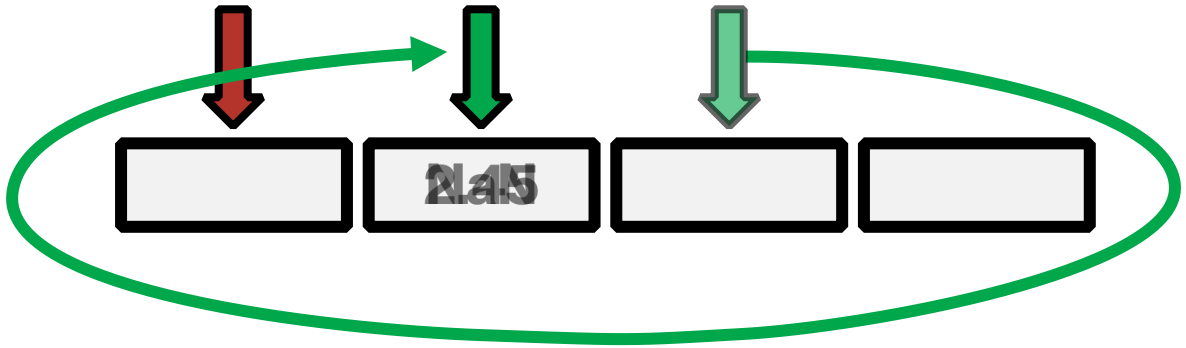
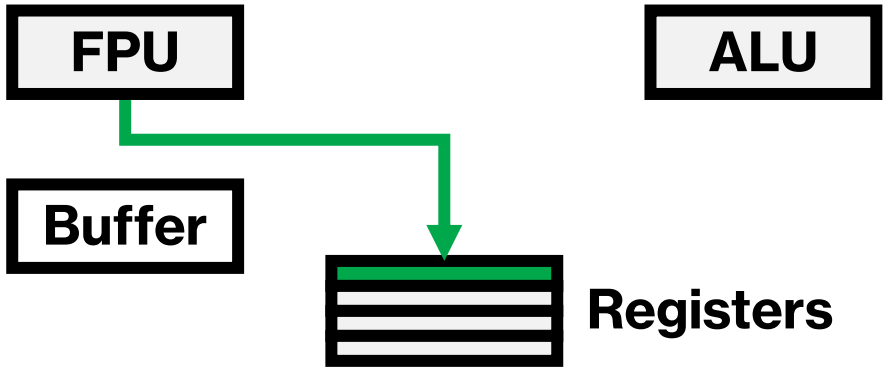


Buffer between FPU and GRs



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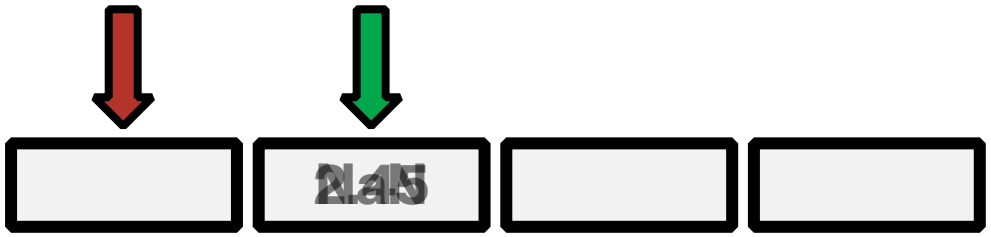
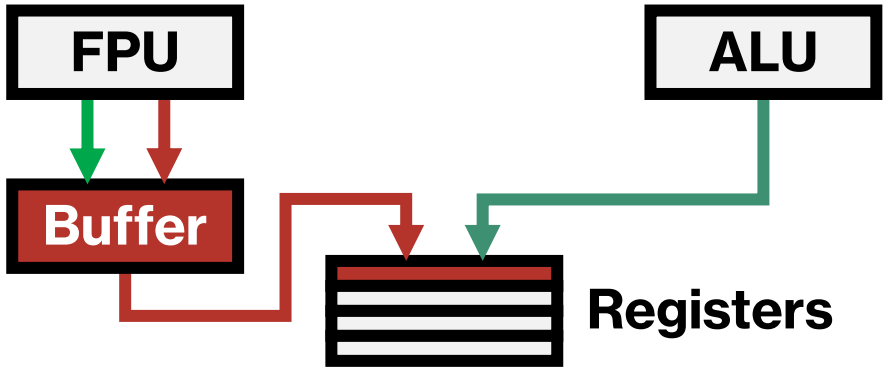


Buffer between FPU and GRs



Insight 6:
Fuzzers often miss subtle bugs from microarchitectural corner cases

Conclusion

- Hardware fuzzing is rife with false theories

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- Hardware fuzzing is rife with false theories
- Accurate evaluation ensures transparency
- Reveals insights into improving future fuzzers