ETH zürich

Pathfinder: Constructing Cycle-accurate Taint Graphs for Analyzing Information Flow Traces

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DVClub Cambridge

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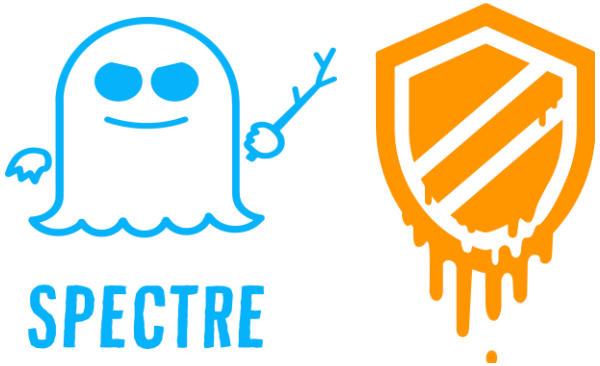
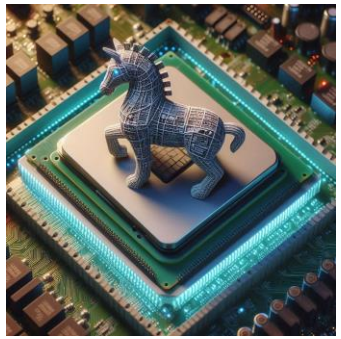
COMSEC

Timing
side channels



Speculative execution
attacks

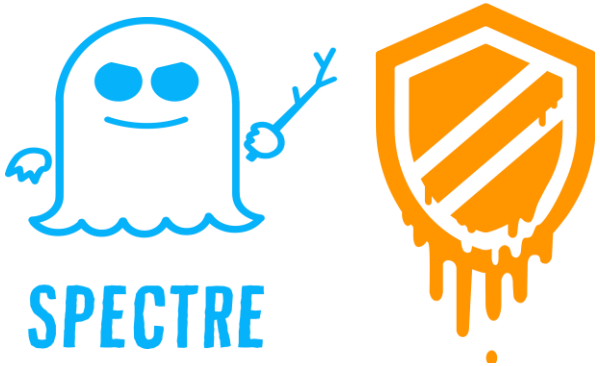


Hardware Trojans

Access control
violations

AI model theft

Timing
side channels



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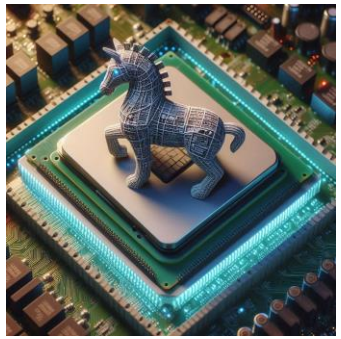

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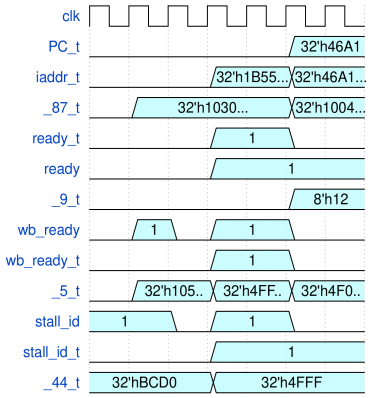

Information
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tracking
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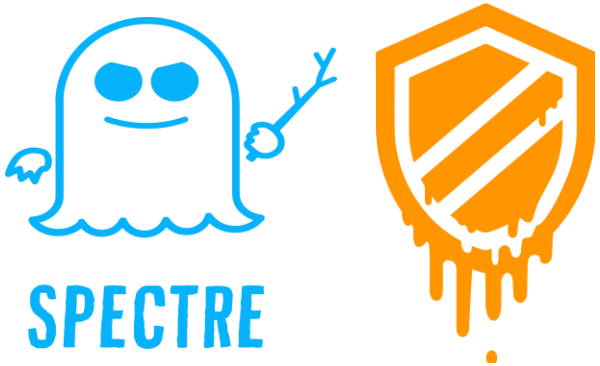

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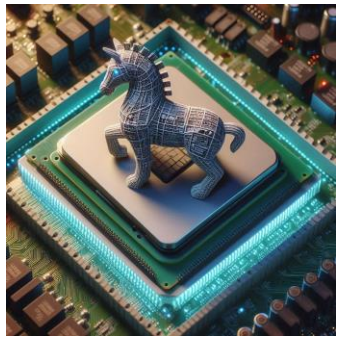

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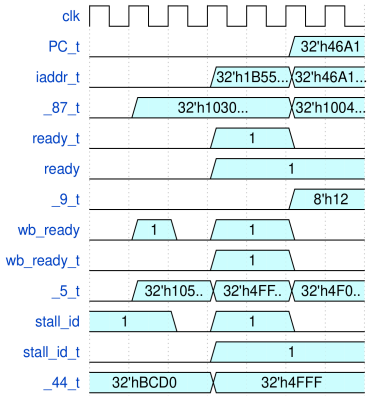

Information
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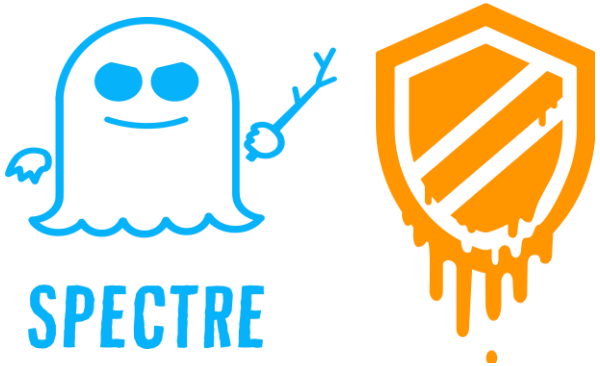
BOOM CPU - Spectre:
17 317 tainted signals

Timing
side channels



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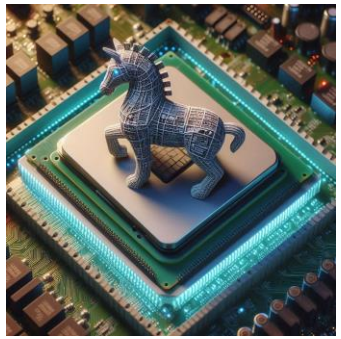

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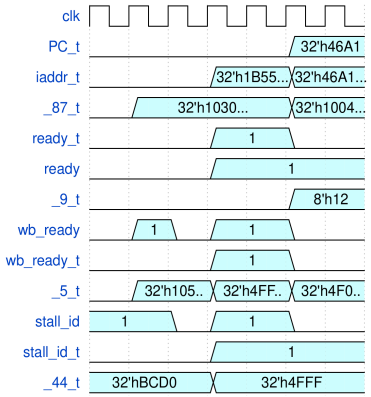

Information
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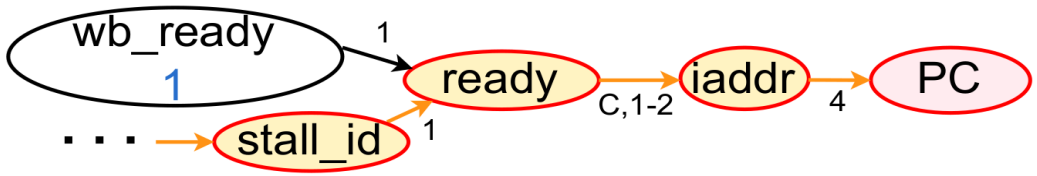
Taint graph



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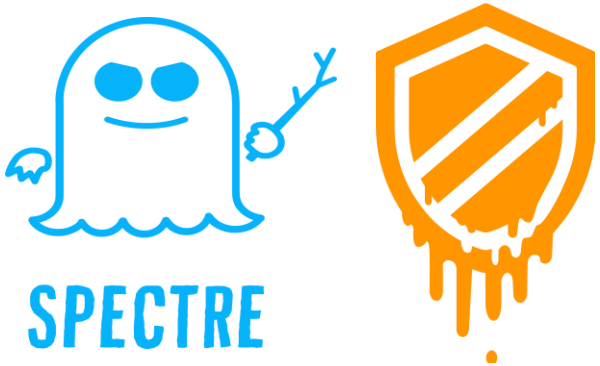

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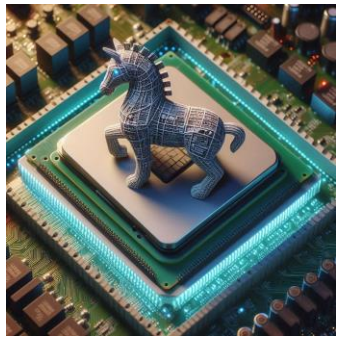

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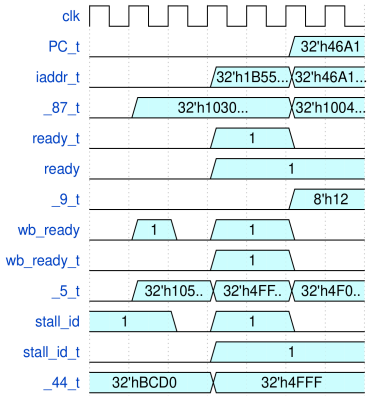

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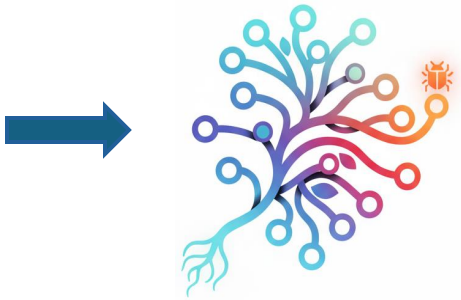
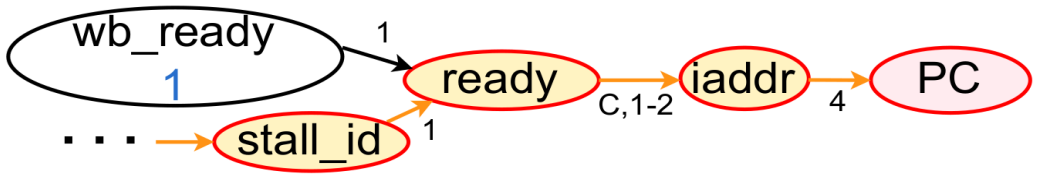


Taint graph

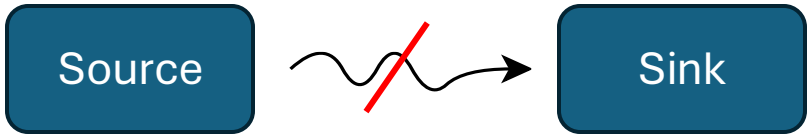


BOOM CPU - Spectre:
17 317 tainted signals

BOOM CPU - Spectre:
213 signals on path

Security Properties

Information flow properties

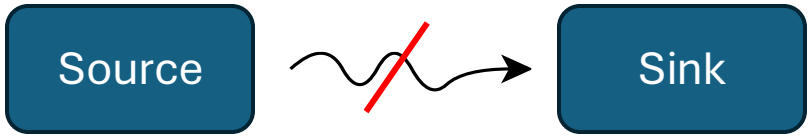


Information =

- data flows
- time & control flows

Security Properties

Information flow properties



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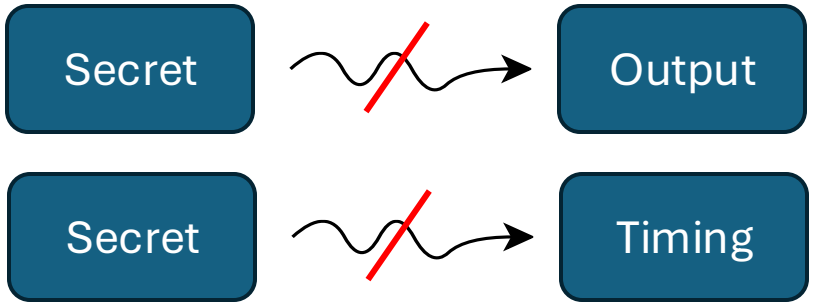
Confidentiality



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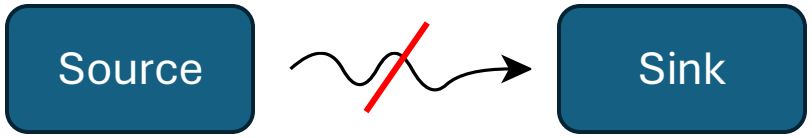

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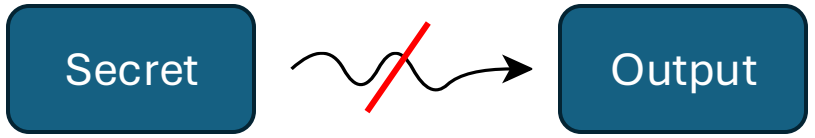
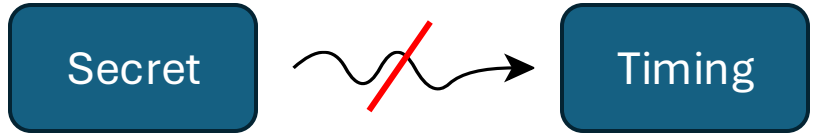
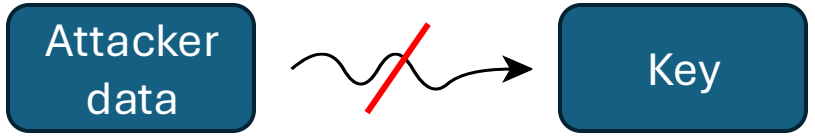
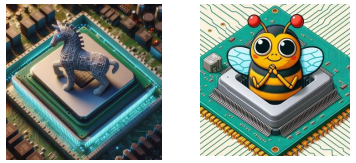




Integrity





Challenges

- Plethora of information flow tracking methods and tools

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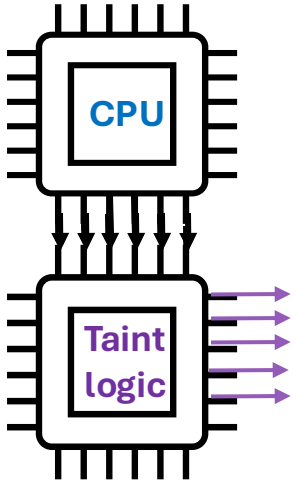

Taint tracking:
GLIFT [8], RTLIFT [9], CellIFT [10], RTL2MμPATH [11], μCFI [12], MileSan [13], …

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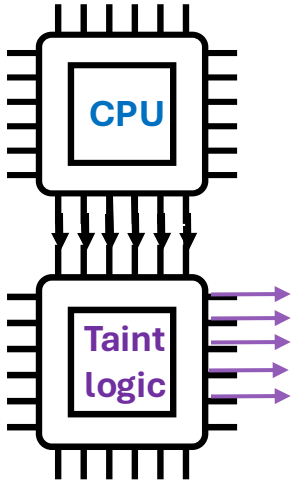

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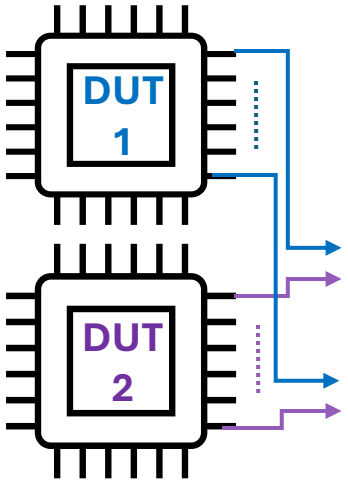
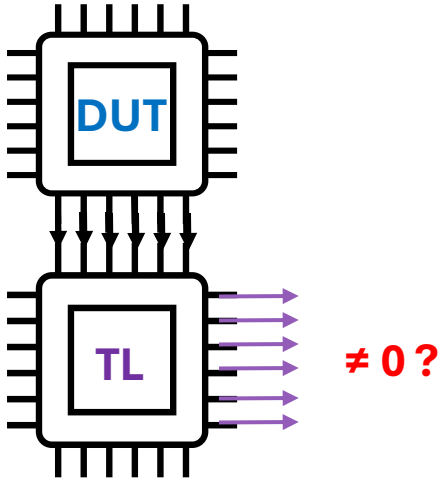


Self-composition / miter:
UPEC [1-3],
AutoCC [4], LeaVe [5],
H-Houdini [6], SPV [7], …

Verifying Information Flows with **Taint Tracking**

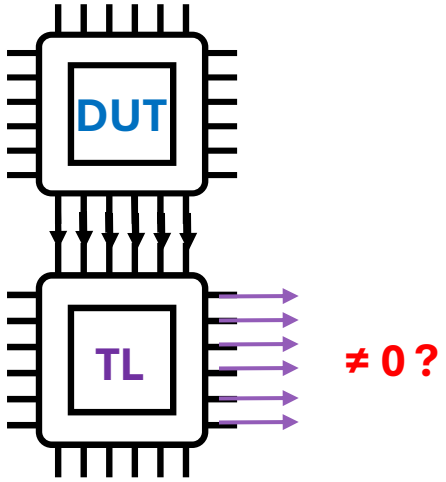


≠ 0 ?

Taint Logic (TL)
tracks information flows

DUT = Design Under Test

Verifying Information Flows with **Taint Tracking**



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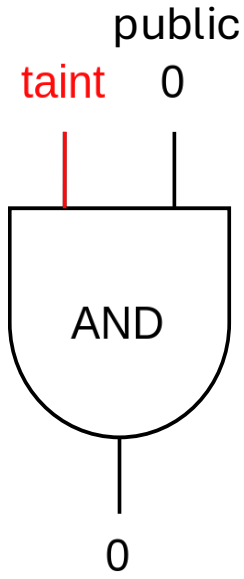

taint = **secret** or **attacker-controlled**

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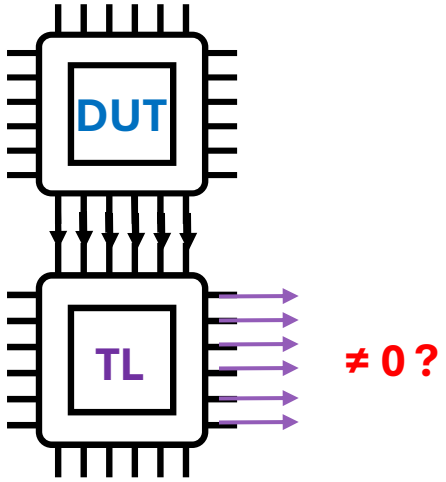

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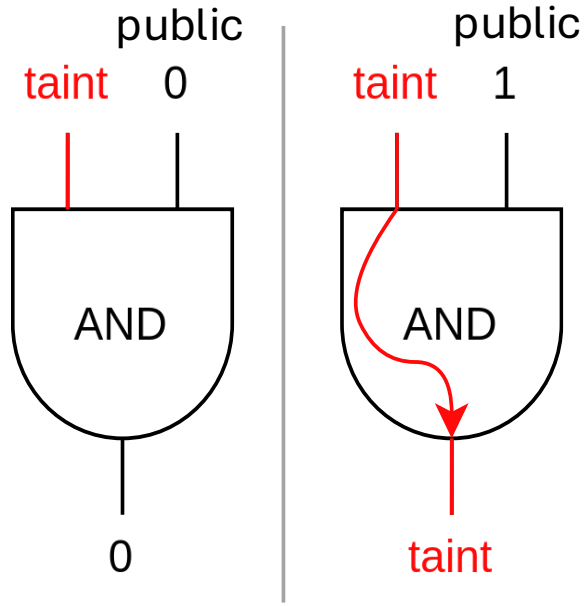

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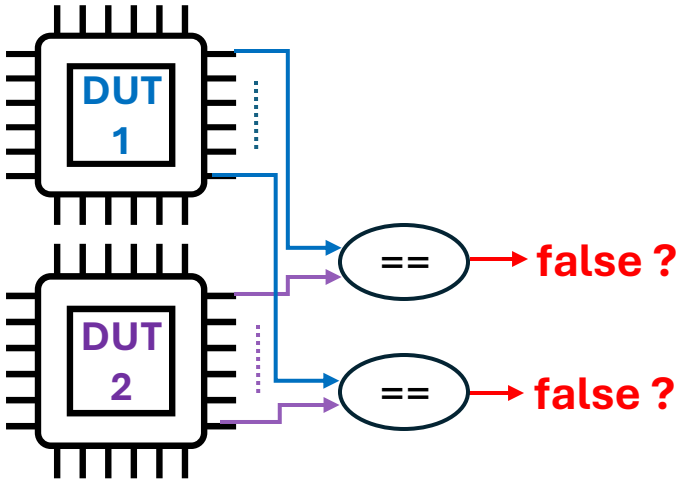
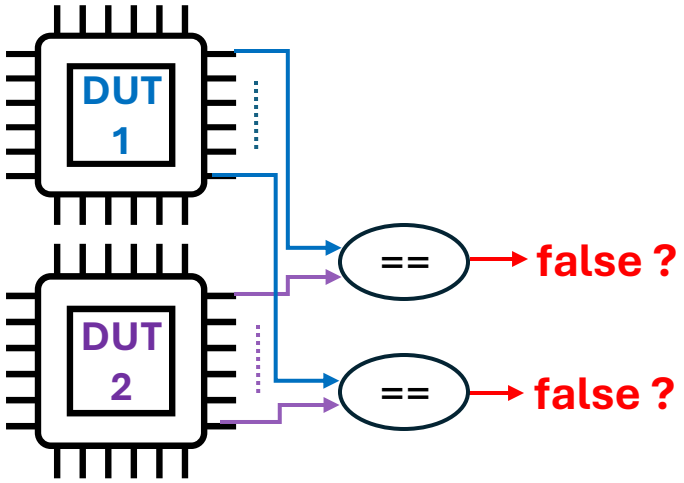


Difference in values
between the two DUT copies
tracks information flows

DUT = Design Under Test

Verifying Information Flows with **Self-composition**



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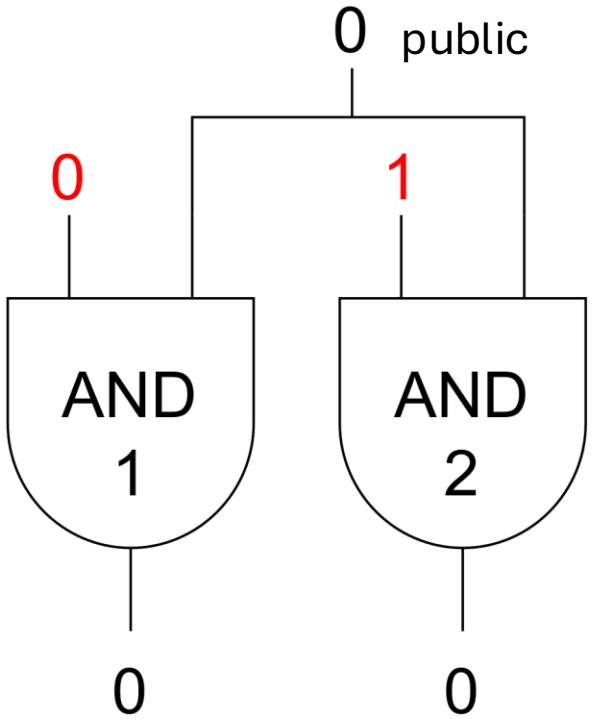

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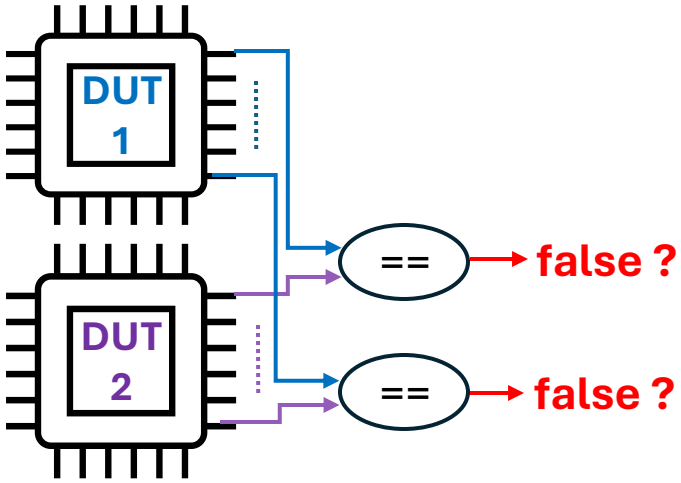

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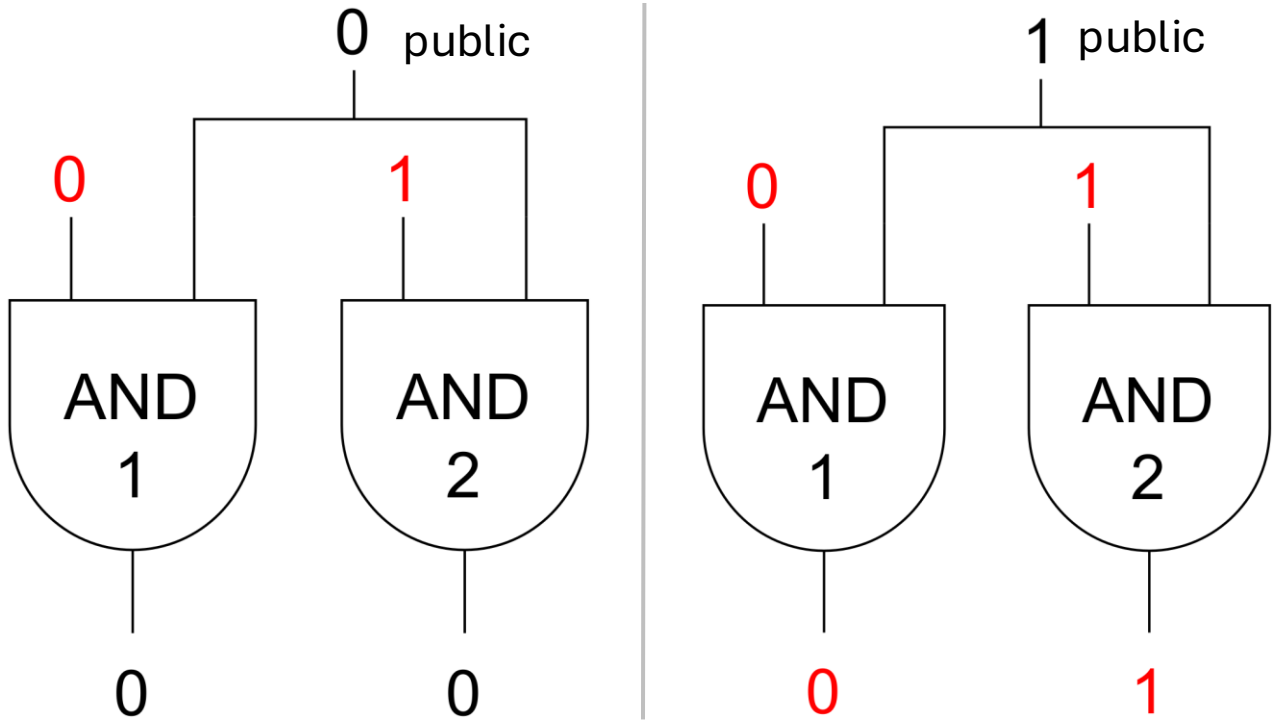

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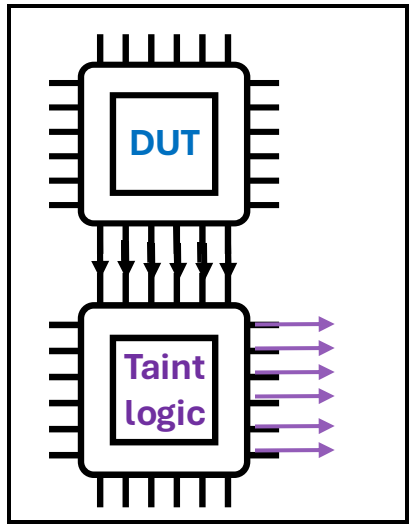
Formal Verification of Information Flows

Taint logic



Formal SVA properties

SVA = SystemVerilog Assertions
DUT = Design Under Test

Formal Verification of Information Flows

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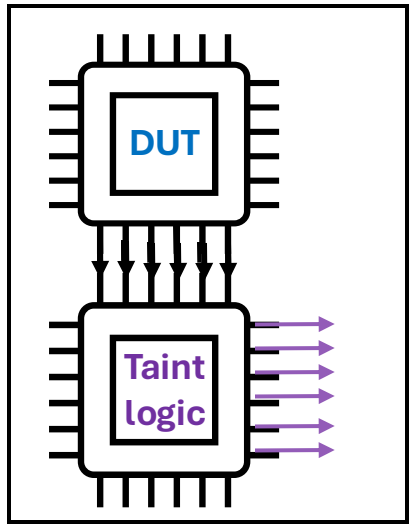

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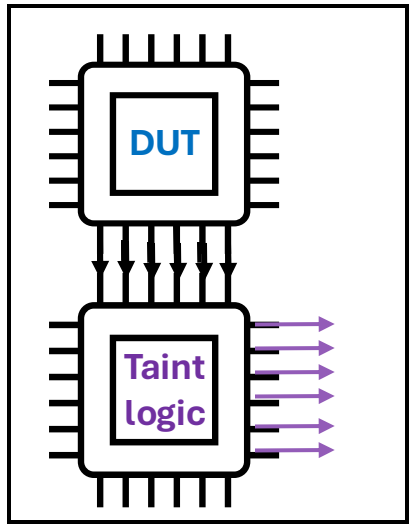

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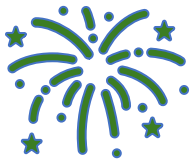
Formal proof



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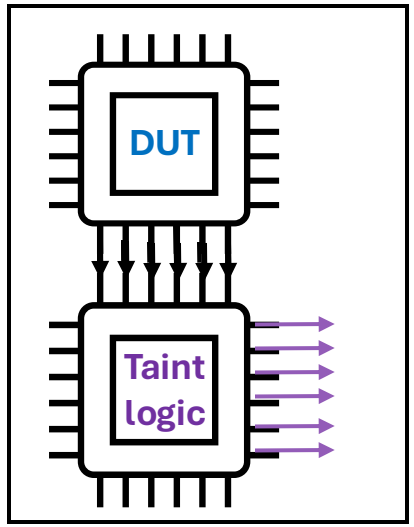

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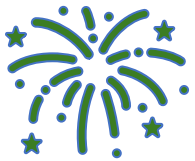
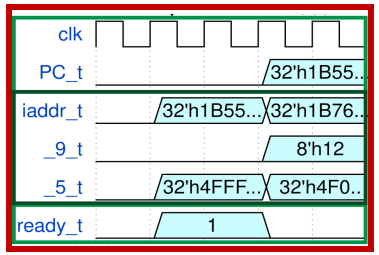


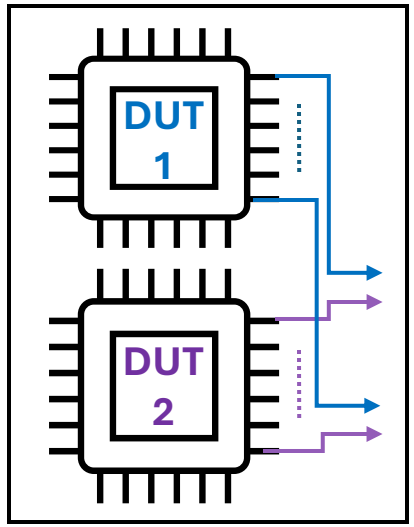
Counter example



Waveform,
e.g., Value Change Dump (VCD)

SVA = SystemVerilog Assertions
DUT = Design Under Test

Formal Verification of Information Flows



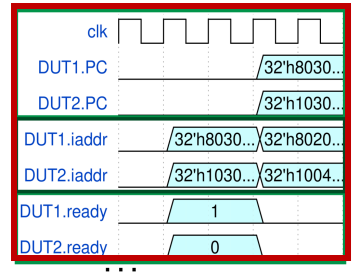
Self-composition / miter

Formal SVA properties

Formal model checker

Formal proof

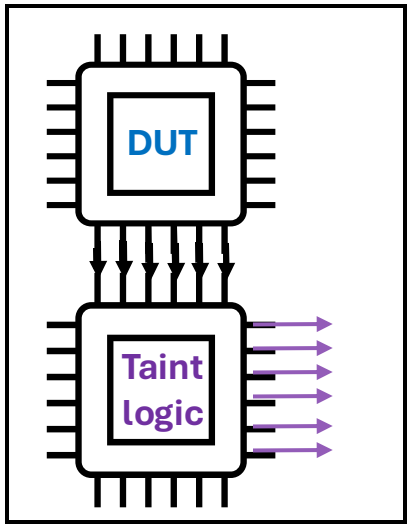
Counter example



Waveform, e.g., Value Change Dump (VCD)

Simulation of Information Flows

Taint logic



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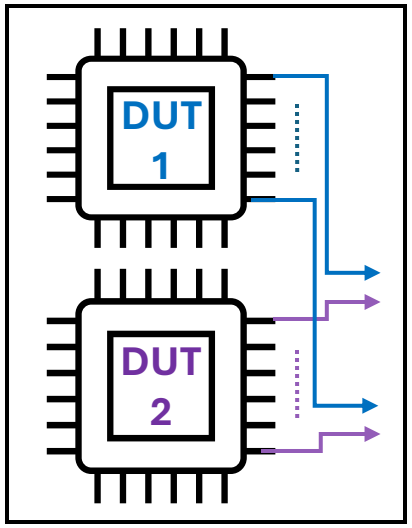
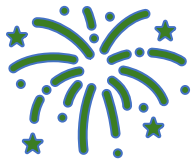
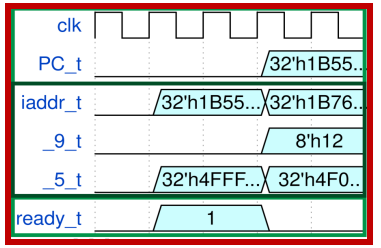


Simulation test benches

Test passes



Test fails

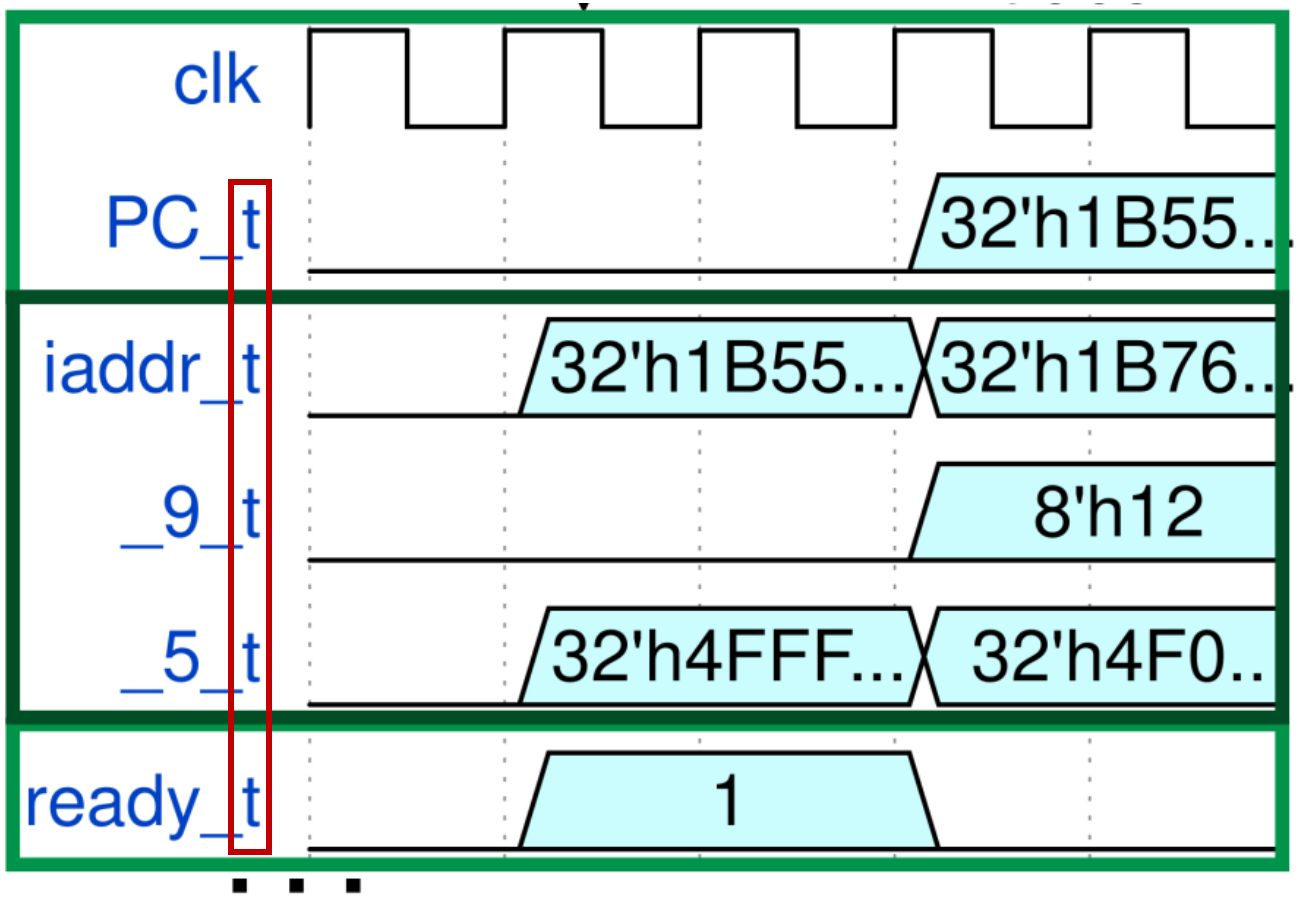


Waveform,
e.g., Value Change Dump (VCD)

Taint Logic Waveform Debugging

```
assign iaddr =
    ready ? ...  : ... ;

always (@posedge clk)
   if (...)
    PC <= iaddr;
```



Self-composition Waveform Debugging

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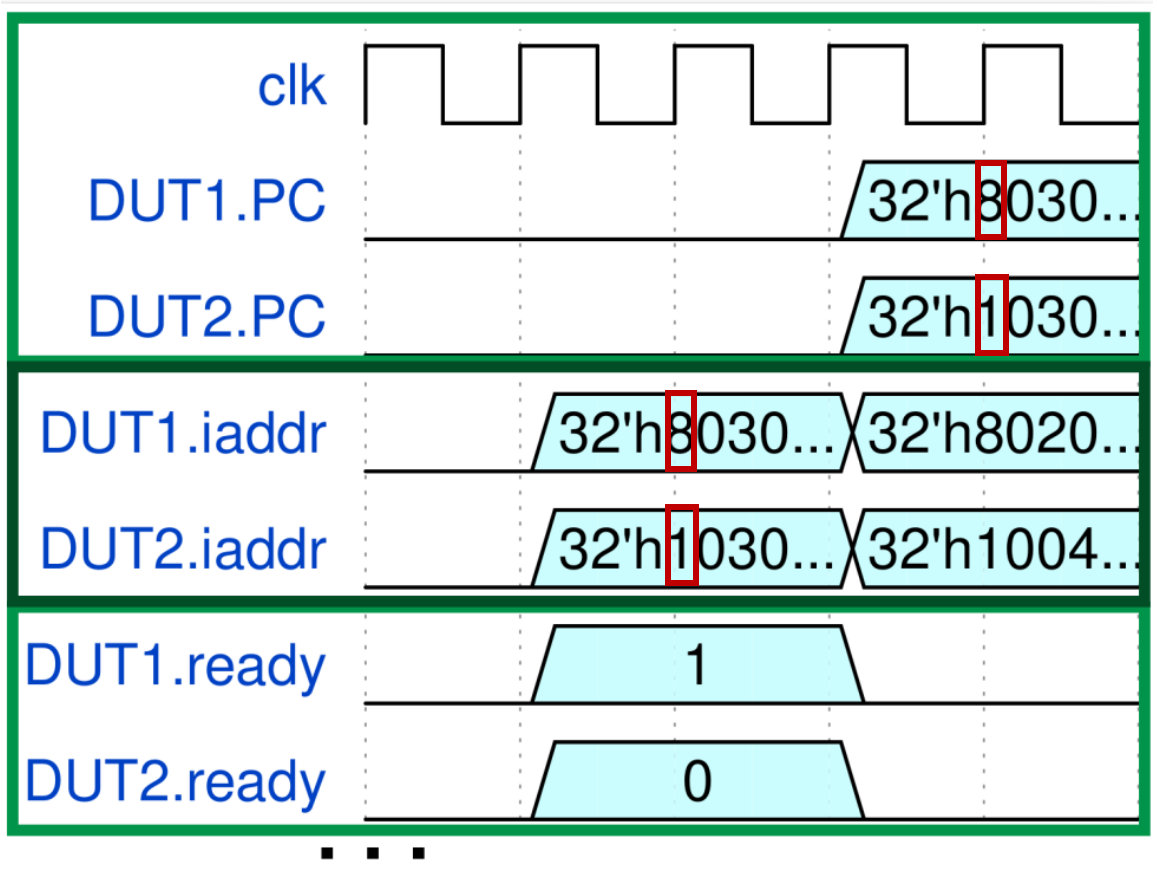
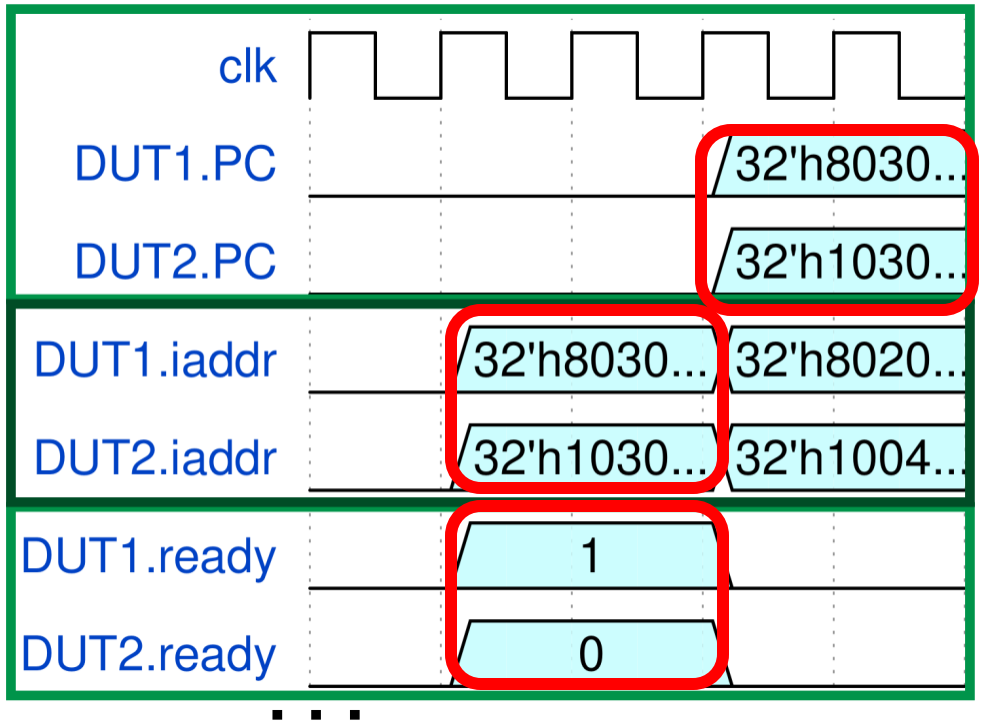
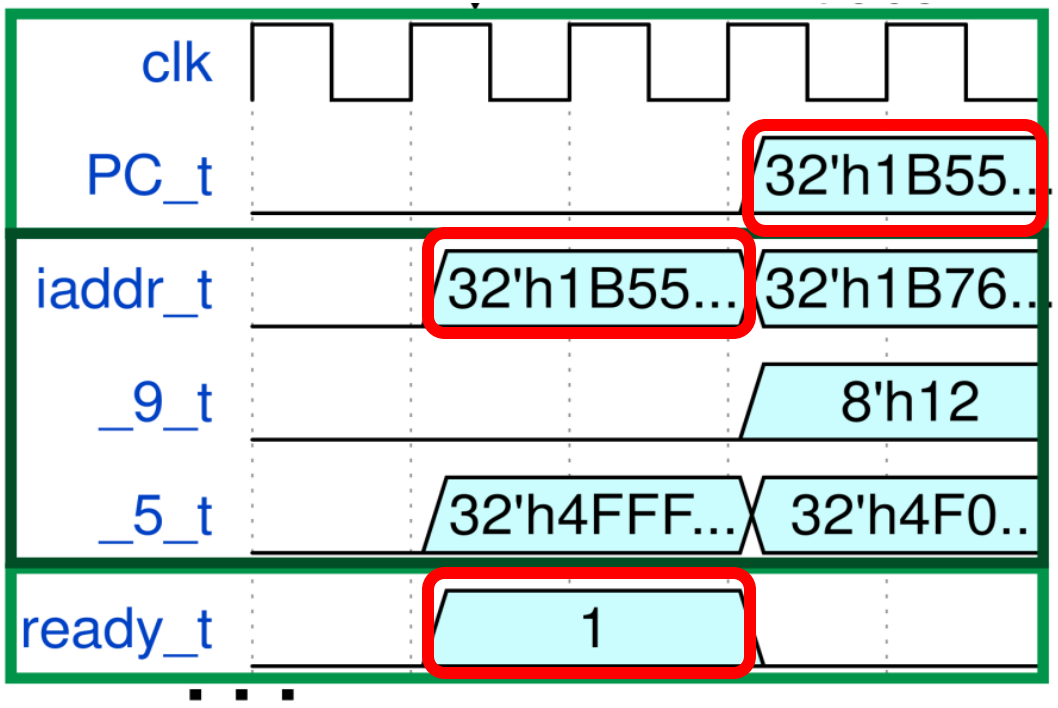
assign iaddr =
    ready ? ...  : ... ;

always (@posedge clk)
   if (...)
    PC <= iaddr;
```



Proof of unification of self-composition and taint tracking





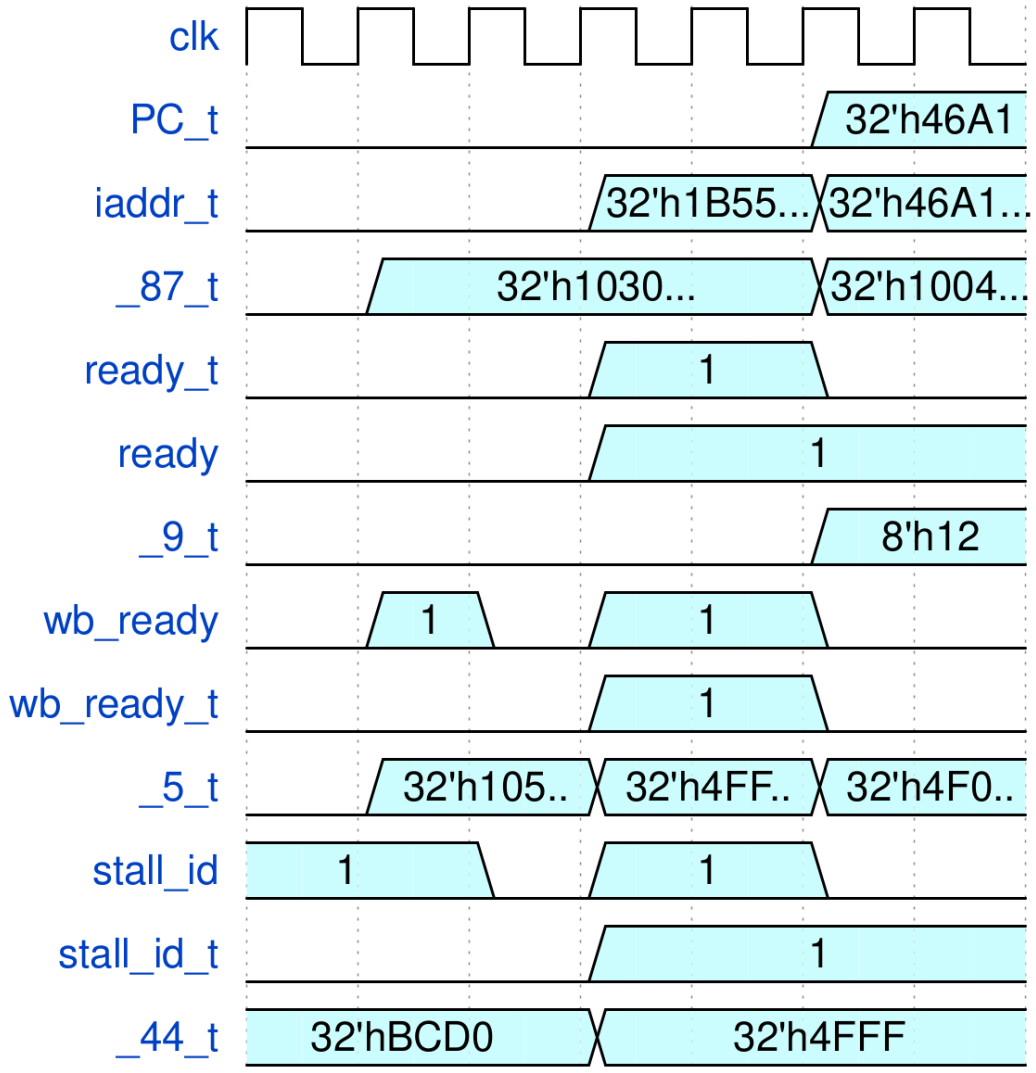
self-composition flow ➡ taint tracking flow

100% precise taint tracking flow ➡ self-composition flow

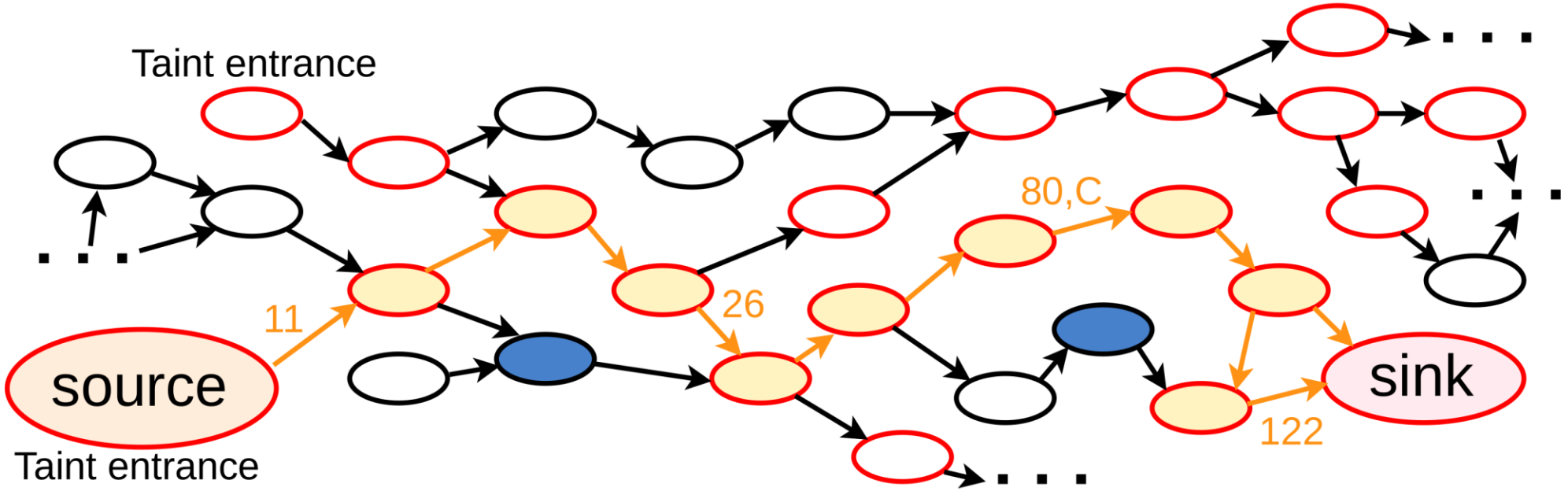
Challenges

- Plethora of information flow tracking methods and tools

- **Functional verification debugging tools show too much information**



Pathfinder



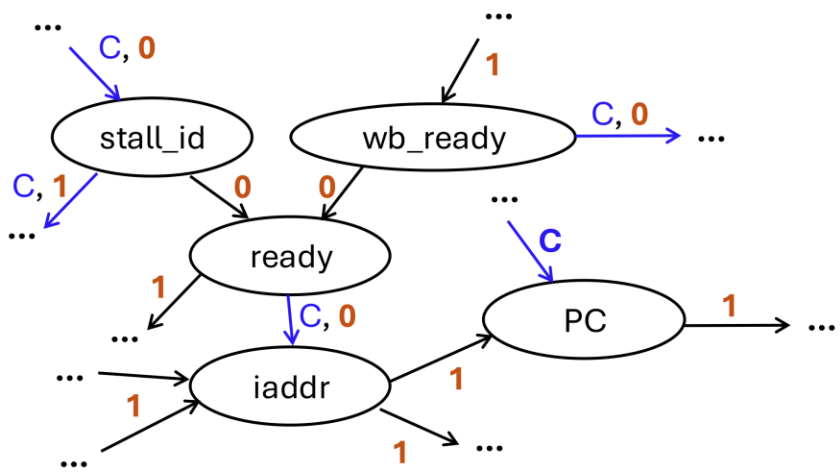
- **Where**, **when** and **why** does information flow?
- Visualizes clock-cycle-accurate propagation of information

Pathfinder - Overview

```
assign iaddr =
    ready ? ...  : ... ;

always (@posedge clk)
   if (...)
    PC <= iaddr;
```

Hardware Description Language (HDL)



Temporal Information Flow Graph (TIFG)

Pathfinder - Overview

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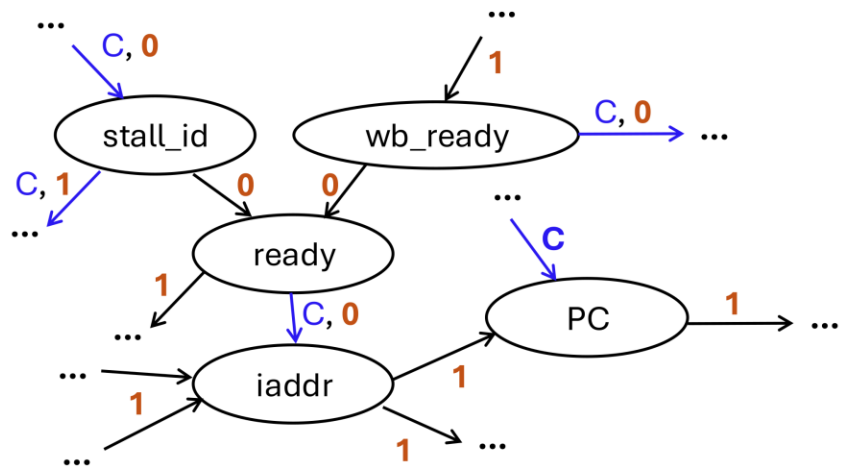
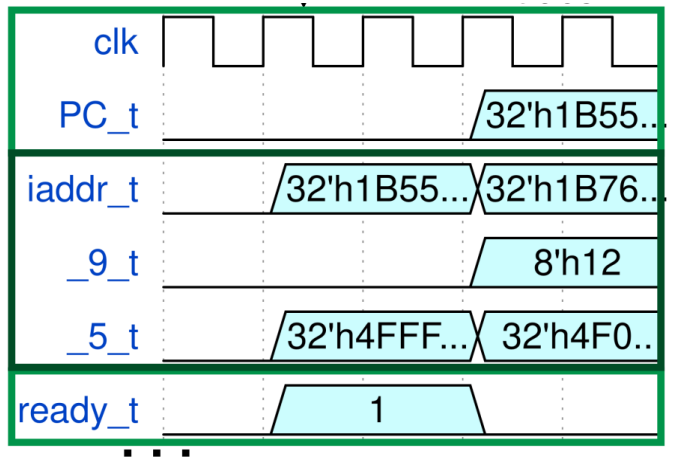


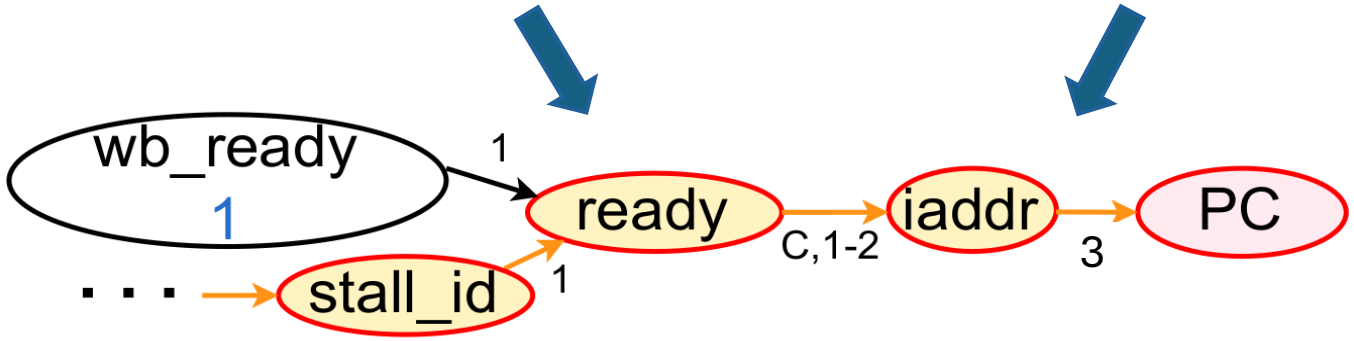
Temporal Information Flow Graph (TIFG)

Formal model checker

Simulation test benches



Waveform (VCD)



Taint Graph (TG)

Pathfinder - Overview

Formal model checker

Simulation test benches

```
assign iaddr =
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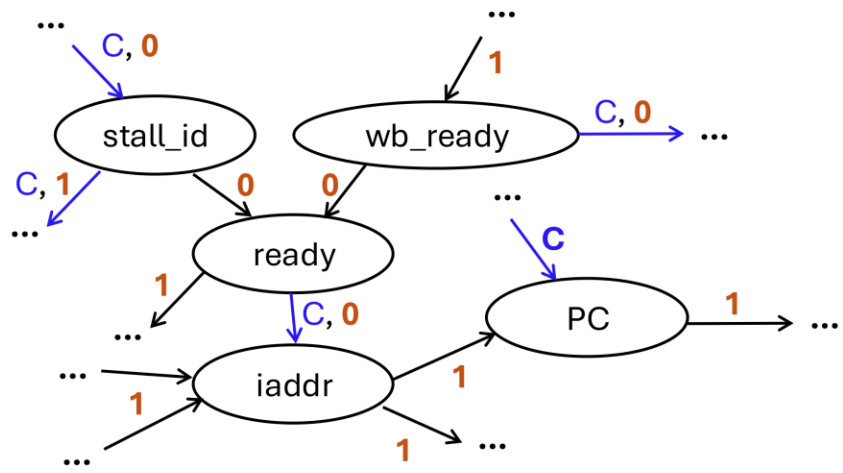
   if (...)
    PC <= iaddr;
```

Hardware Description Language (HDL)



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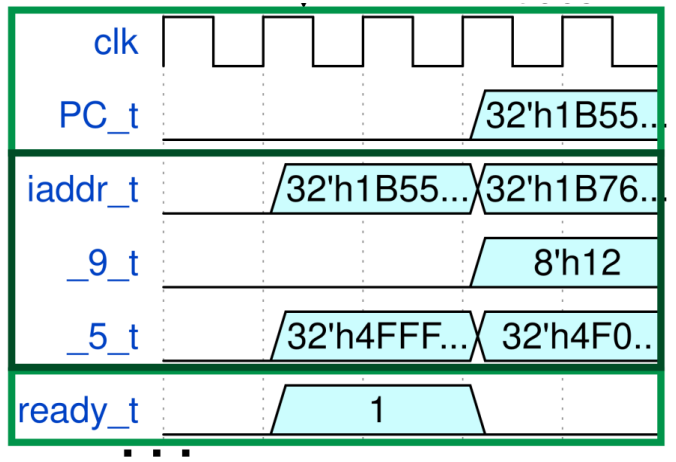

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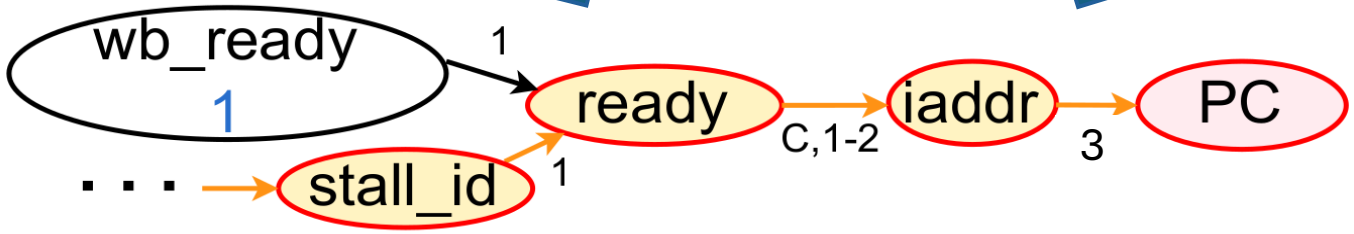

Taint Graph (TG)

Pathfinder - TIFG

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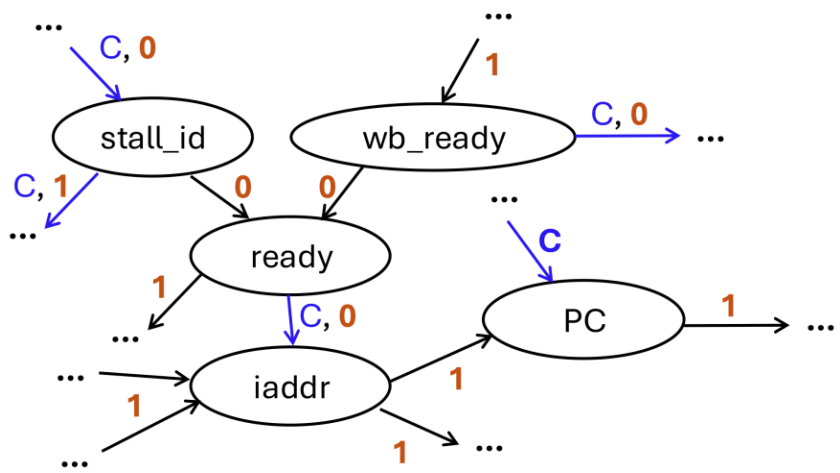
Hardware Description Language (HDL)

TIFG Yosys pass



Temporal Information Flow Graph (TIFG)

[1] Yosys Open SYnthesis Suite - https://github.com/YosysHQ/yosys

Temporal Information Flow Graph (TIFG)

```
assign ready =
    ~stall_id & wb_ready;

assign iaddr =
    ready ? ...  : ... ;

always (@posedge clk)
   if (...)
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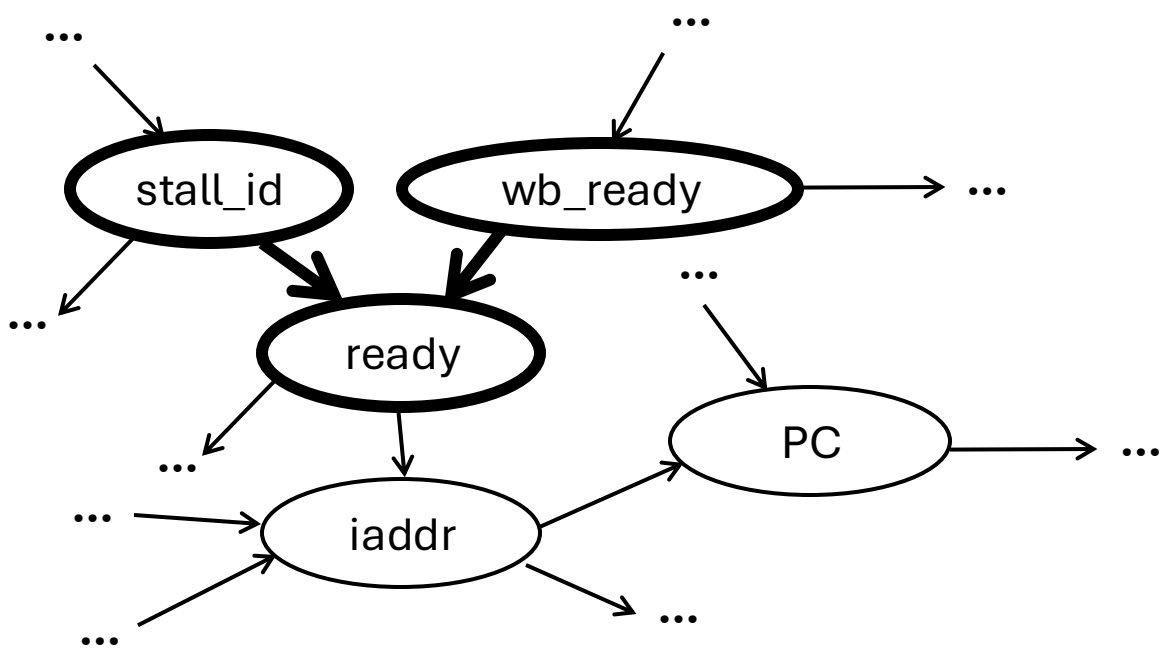
```



encodes **potential information flows**

Temporal Information Flow Graph (TIFG)

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assign ready =
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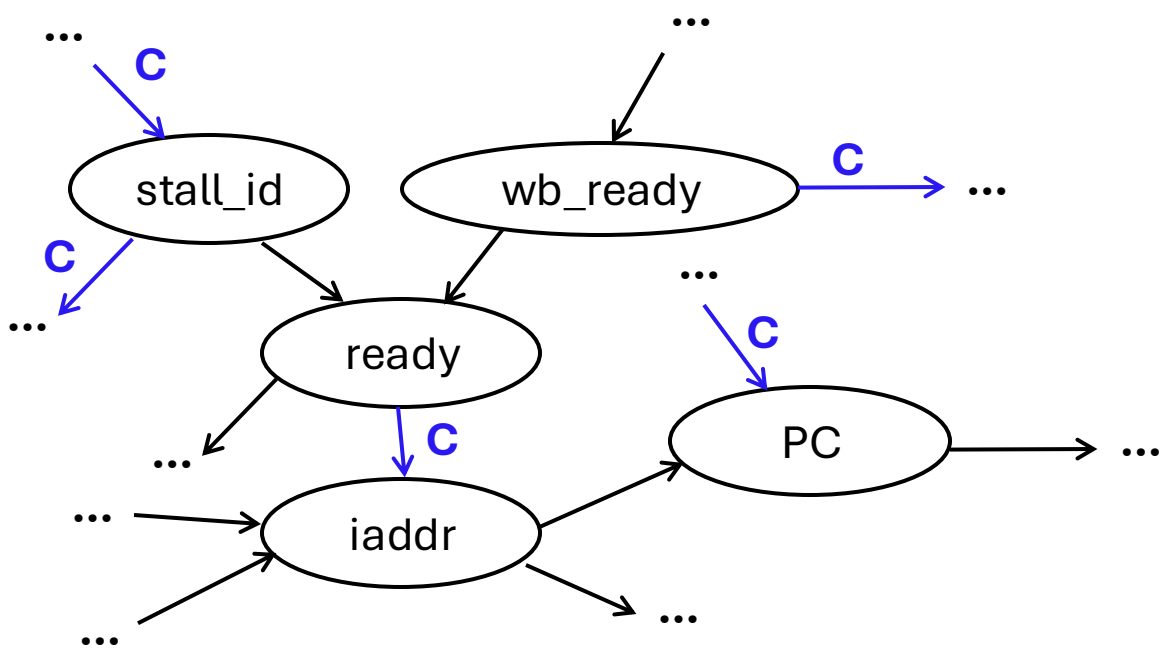

encodes **potential information flows**

C (control) = **implicit** information flow

Temporal Information Flow Graph (TIFG)

```
assign ready =
    ~stall_id & wb_ready;
```

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assign iaddr =
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   if (...)
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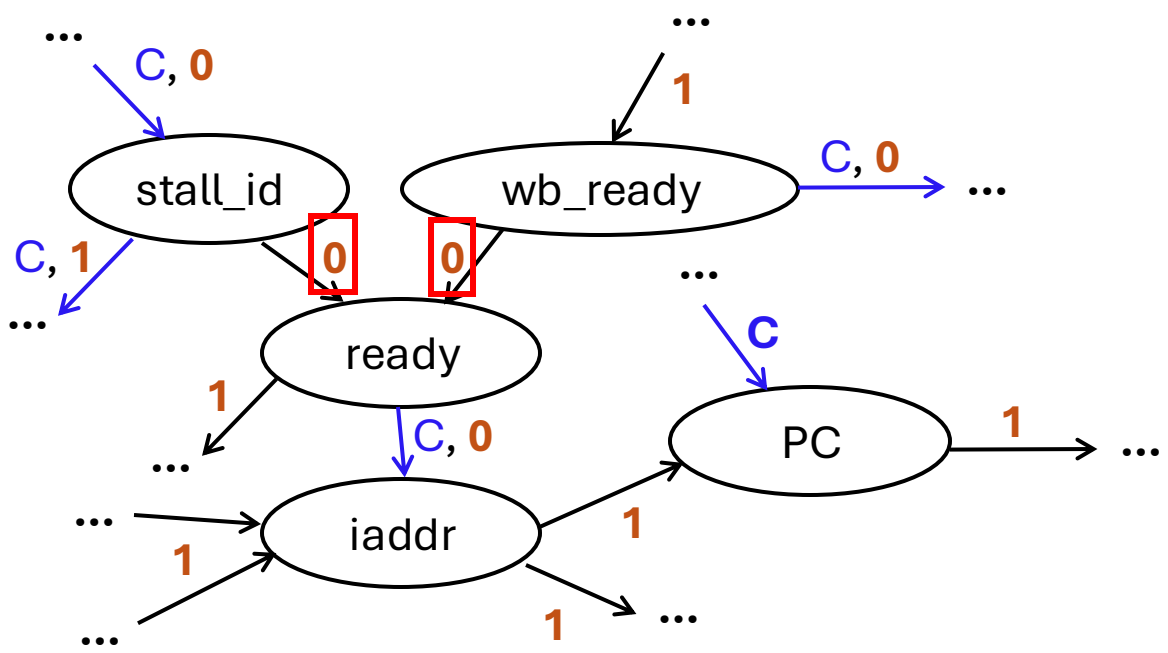

encodes **potential information flows**

C (control) = **implicit** information flow

Nr. = clock cycle **delay**

Temporal Information Flow Graph (TIFG)

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assign ready =
    ~stall_id & wb_ready;

assign iaddr =
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always (@posedge clk)
   if (...)
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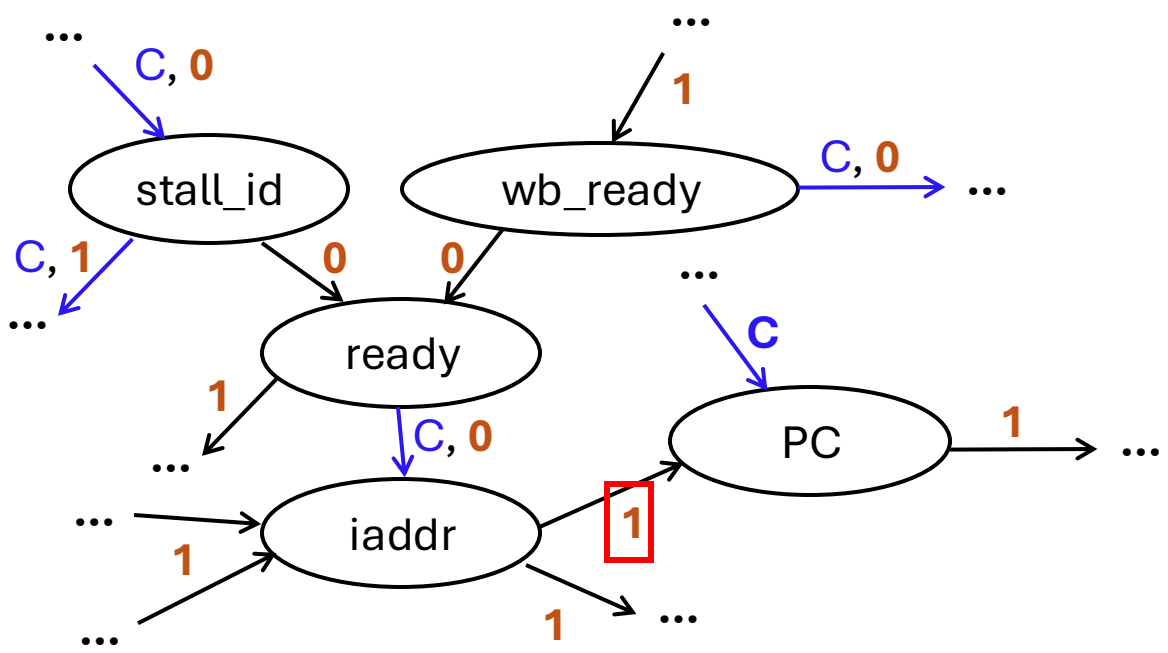

encodes **potential information flows**

C (control) = **implicit** information flow

Nr. = clock cycle **delay**

Pathfinder - Overview

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assign iaddr =
    ready ? ...  : ... ;

always (@posedge clk)
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    PC <= iaddr;
```
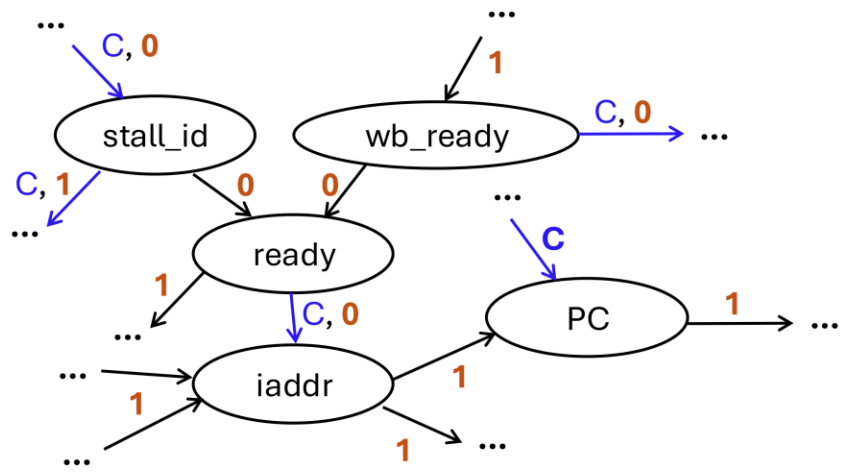
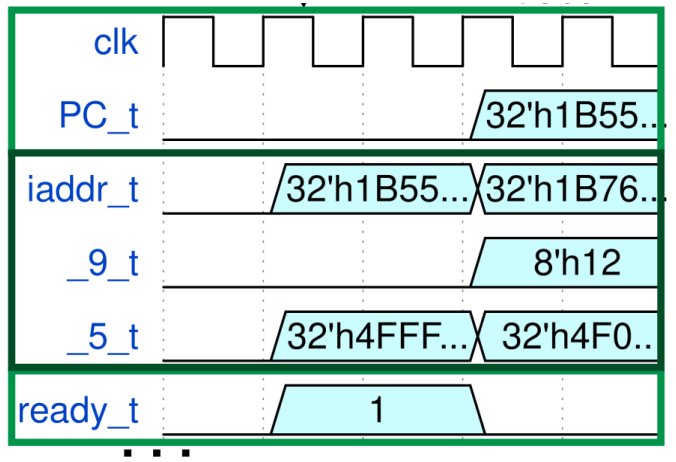

Hardware Description Language (HDL)



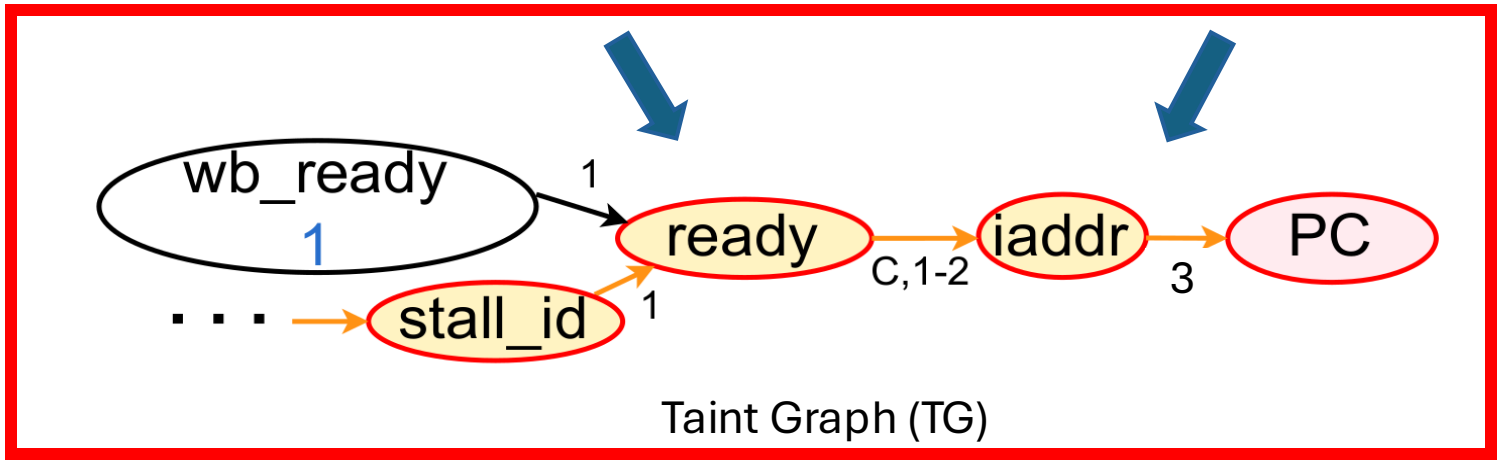
Temporal Information Flow Graph (TIFG)

Formal model checker

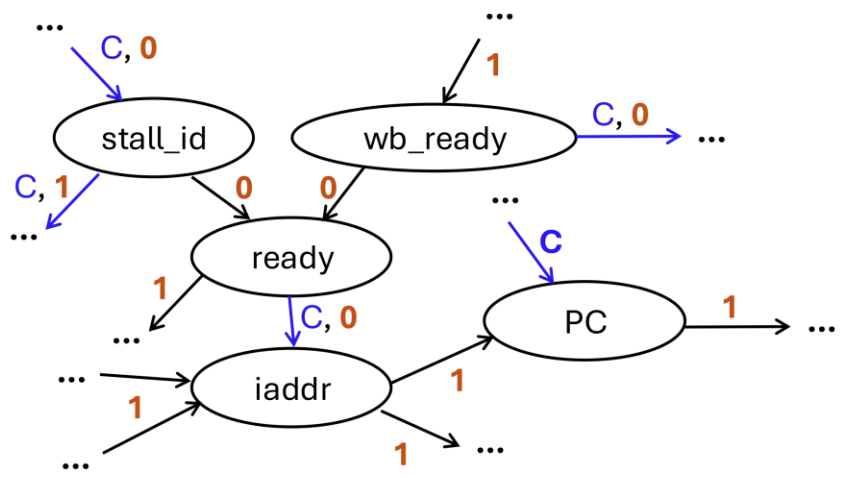
Simulation test benches



Waveform (VCD)



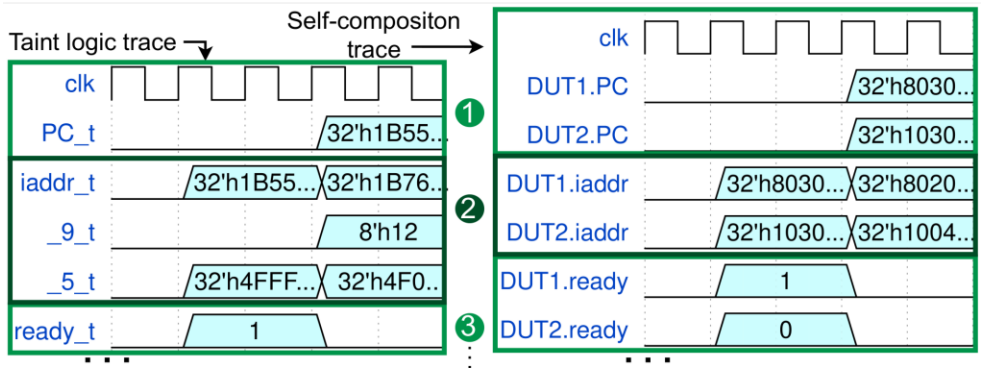
Taint Graph (TG)



Temporal Information Flow Graph (TIFG)

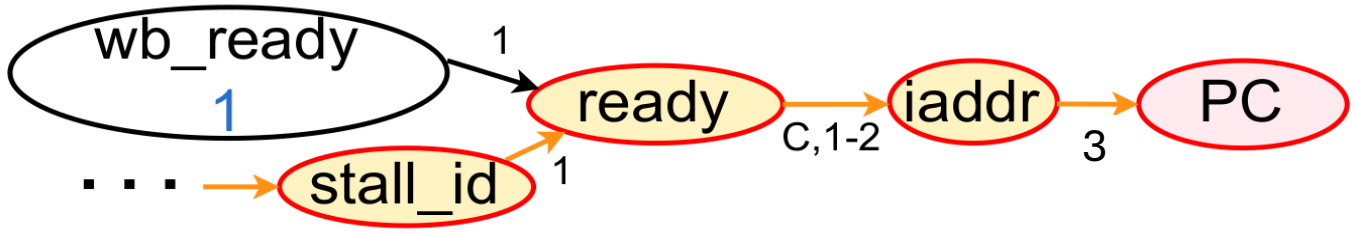
Formal model checker

Simulation test benches

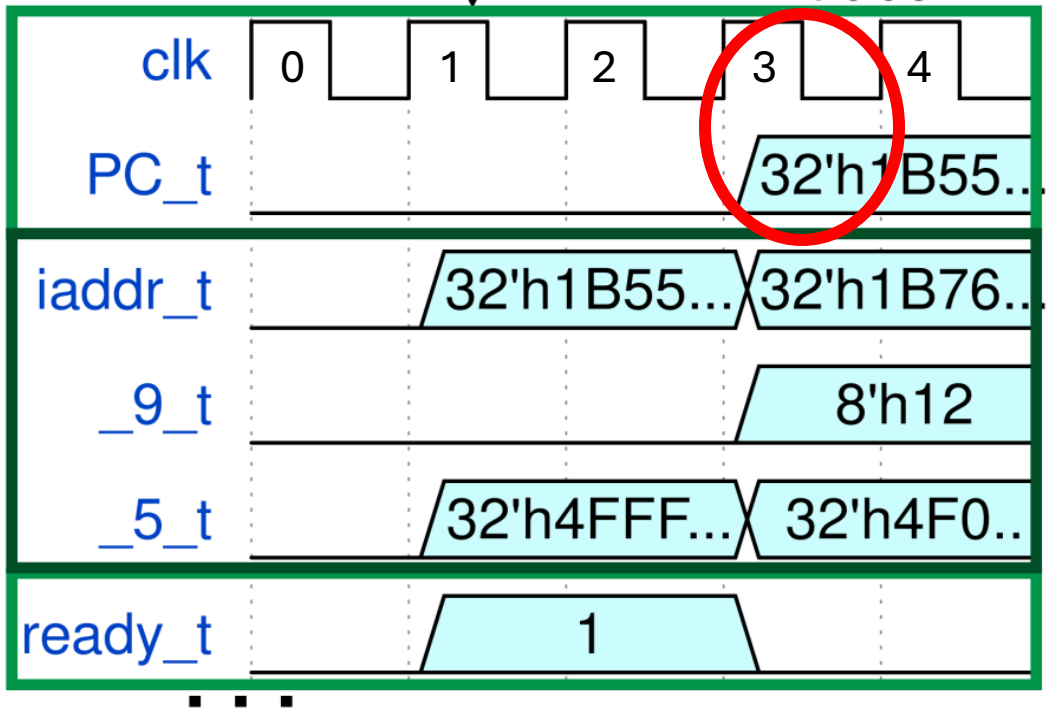


Pathfinder derives **taint** values from **differences** in self-composed design

Pathfinder



Taint Graph (TG)



Pathfinder

Taint Graph construction

Input: waveform, TIFG, taint source/sinks

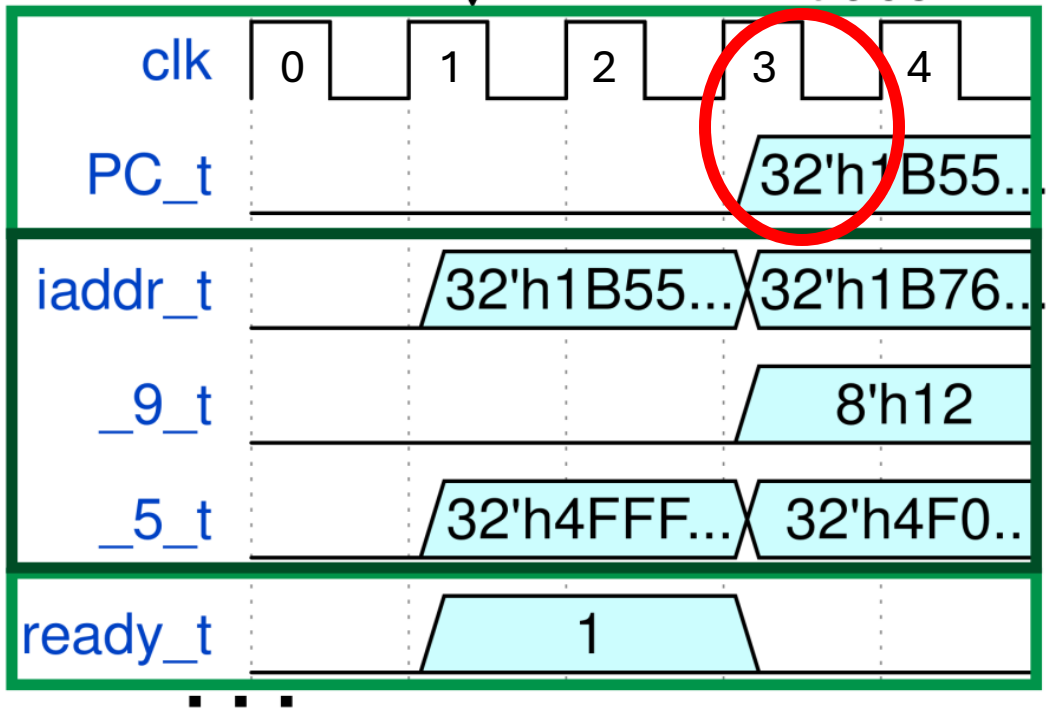
taint sink

PC

Signal 'PC' is first tainted in clock cycle 3

Temporal Information Flow Graph (TIFG)

Pathfinder



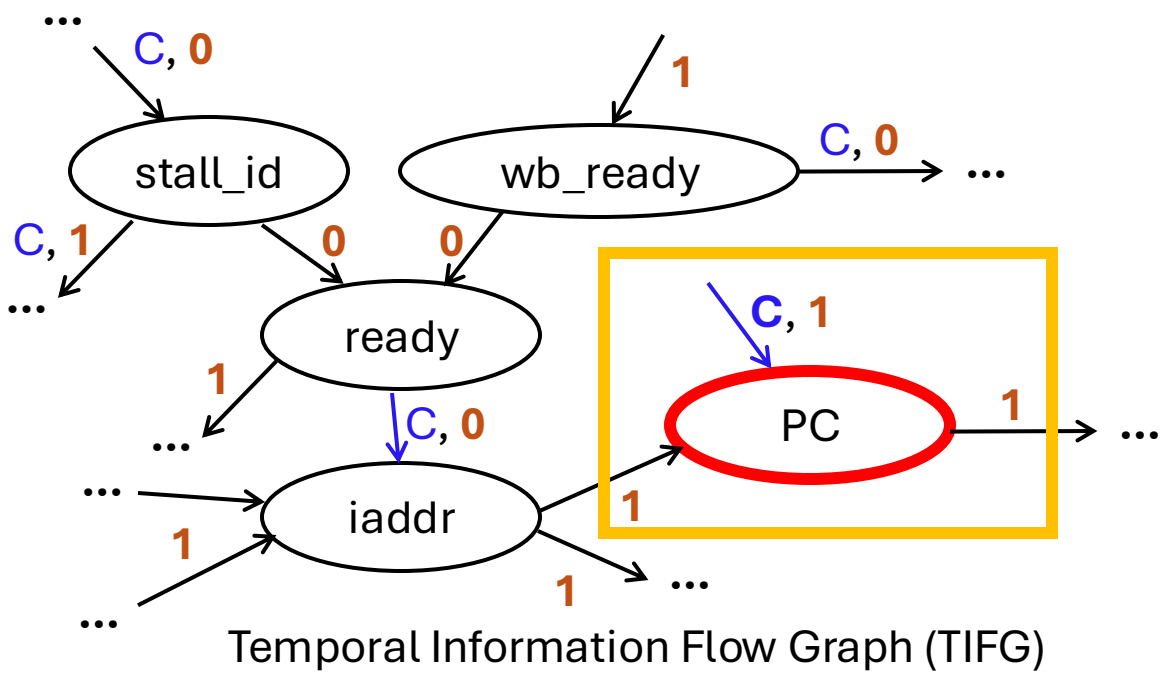
Taint Graph construction

Drivers with zero delay?

No.

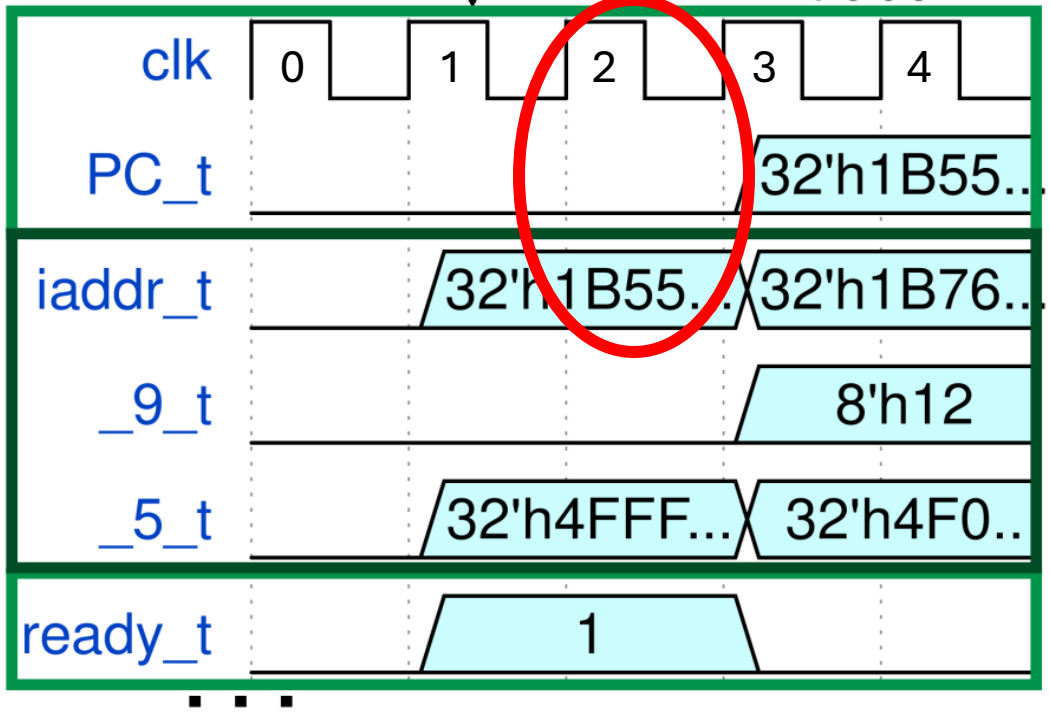
taint sink

PC



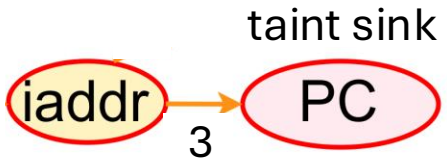
Temporal Information Flow Graph (TIFG)

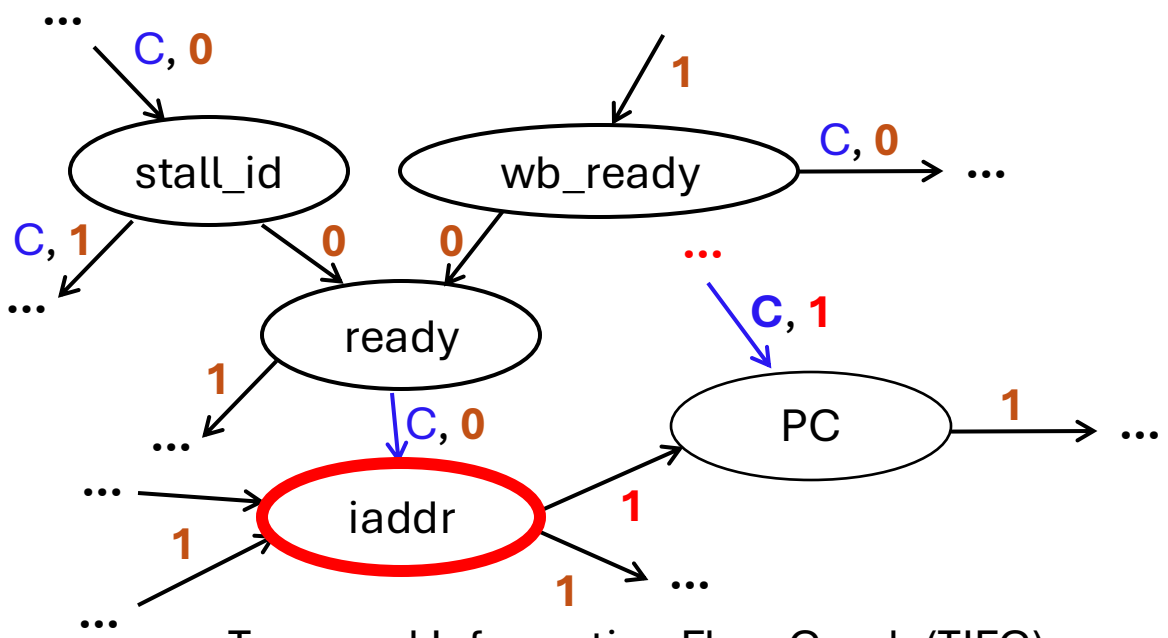
Pathfinder



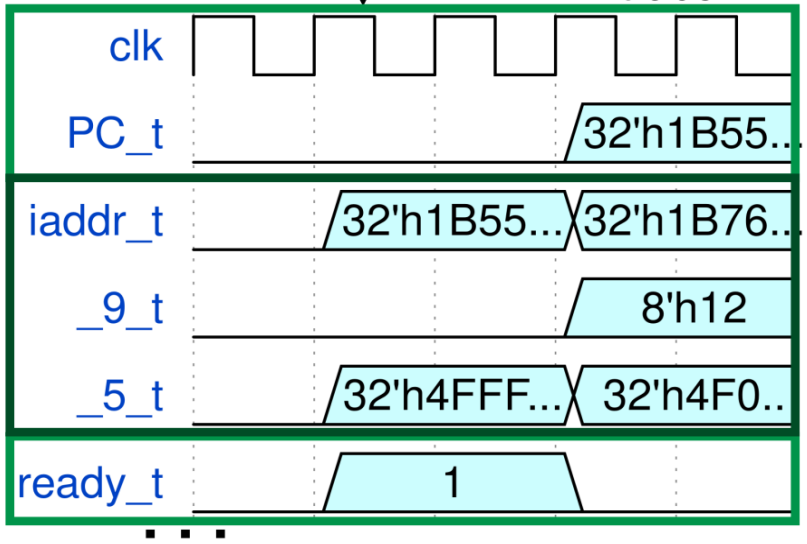
Taint Graph construction

Drivers with 1 cycle delay?
Yes.



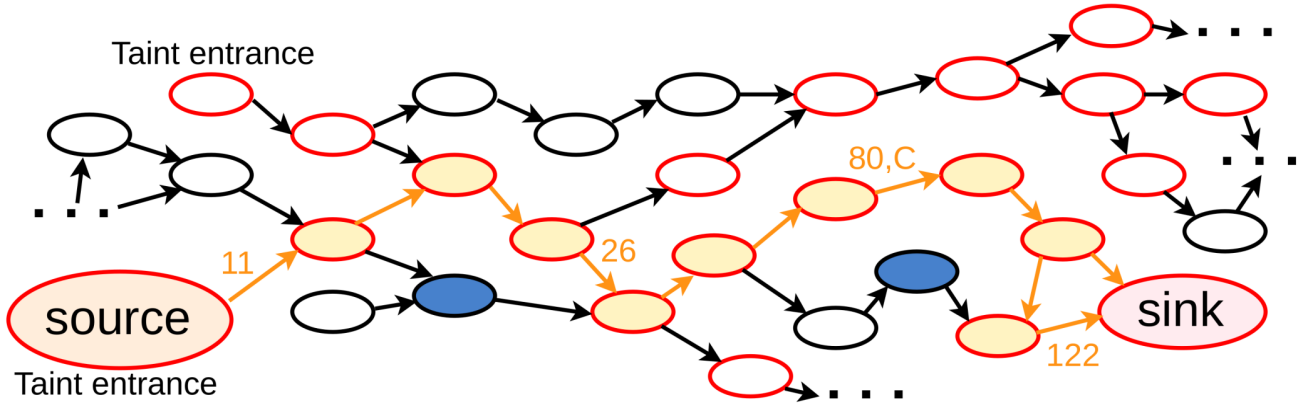


Temporal Information Flow Graph (TIFG)

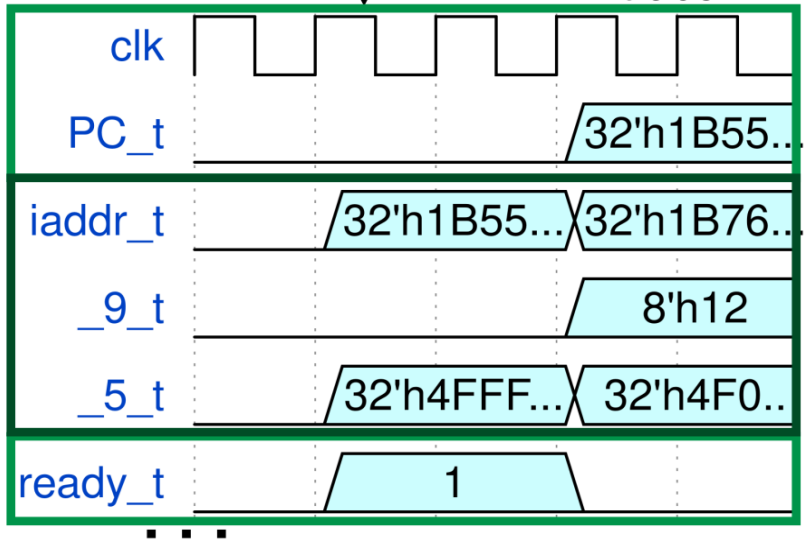


Taint Graph construction

Repeat from source, intersect



Pathfinder



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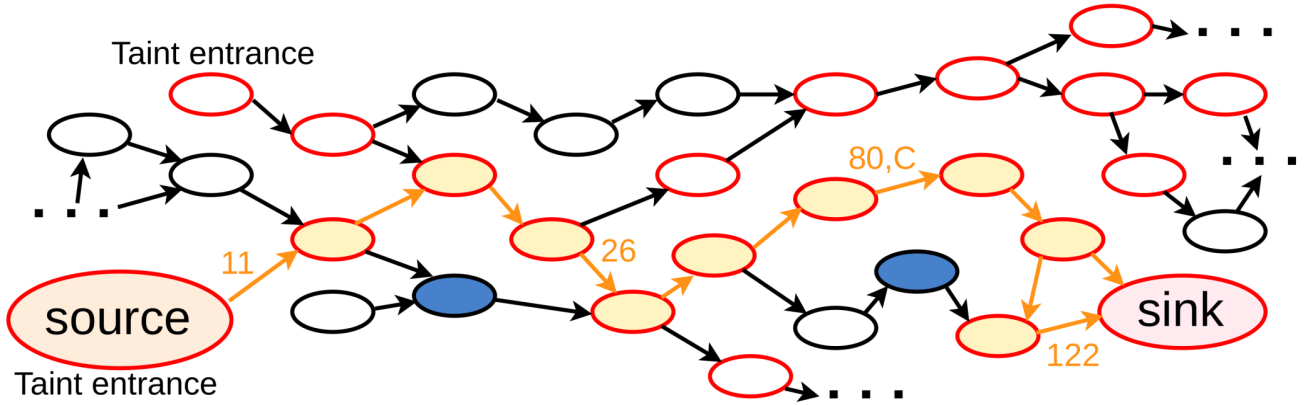
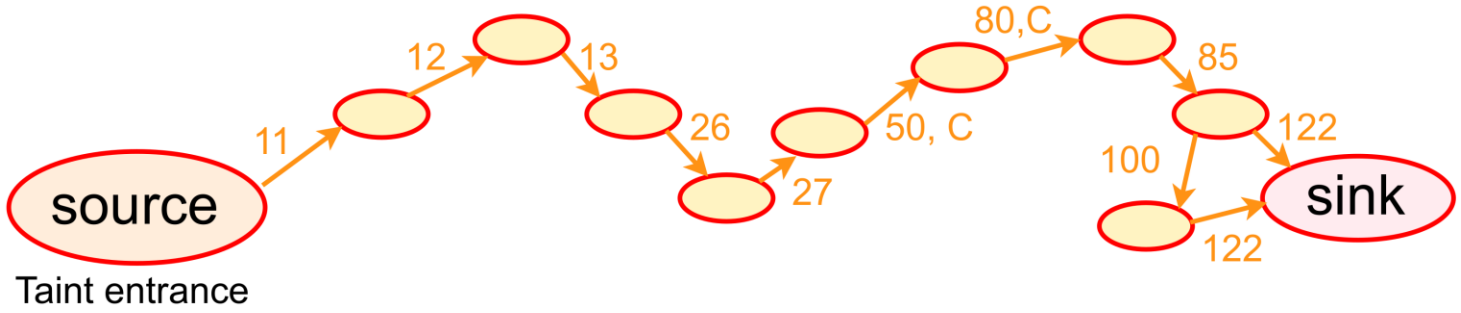


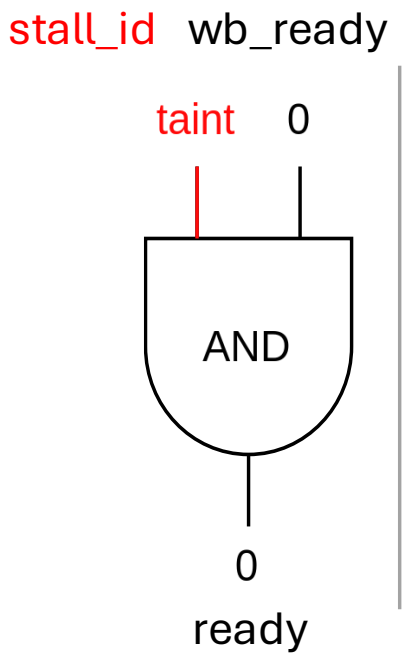
Isolated Taint Graph

Where/when did information flow?



Flow Control Signals

```
assign ready =
    ~stall_id & wb_ready;
```



Why did information flow?

Flow control signal: wb_ready

Flow control condition (wb_ready == 0) blocks information flow

3

Flow Control Signals

```
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```
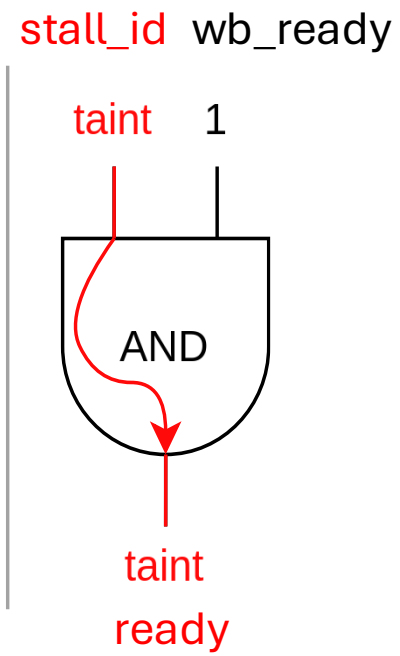
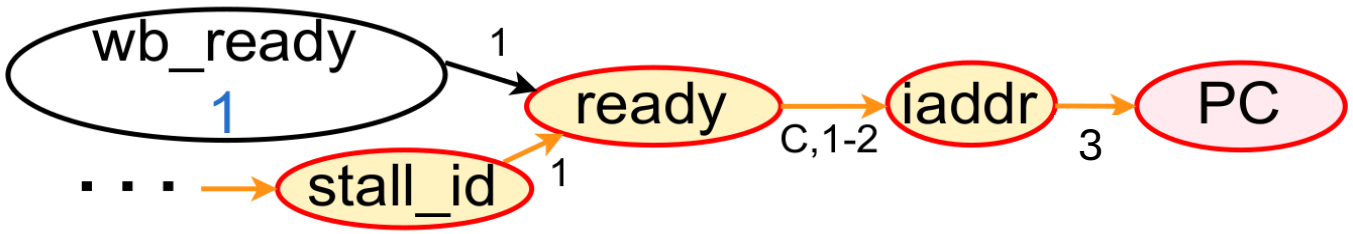



Why did information flow?

Flow control signal: wb_ready

Flow control condition (wb_ready == 0) is false



Results

Design	IFT	Analysis type	Graph type	Tainted signals	Signals on path	Reduct. factor	Clock cycles	Gen. time [s]
AES-400 [15]	TT	Simulation	Path	15	3	5.0	1	6.03
Kronos [5]	TT	Formal	Path	48	19	2.5	9	0.20
Ibex custom [5]	TT	Formal	Path	330	76	4.3	18	0.59
Ibex small [5]	TT	Formal	Path	164	89	1.8	12	0.78
CVA6 (new trace)	TT	Simulation	Path	82,920	1187	769.9	144	604.0
CVA6 [19]	SC	Formal	Bottom	900	562	1.6	76	4.47
BOOM [17]	TT	Simulation	Path	17,316	213	81.3	988	100.93

Pathfinder supports waves of

- self-composition
- taint tracking
- simulation
- formal verification

IFT = Information Flow Tracking, TT = Taint Tracking, SC = Self-Composition

Results

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Number of signals that need to be manually analyzed is reduced by up to ~700x

Results

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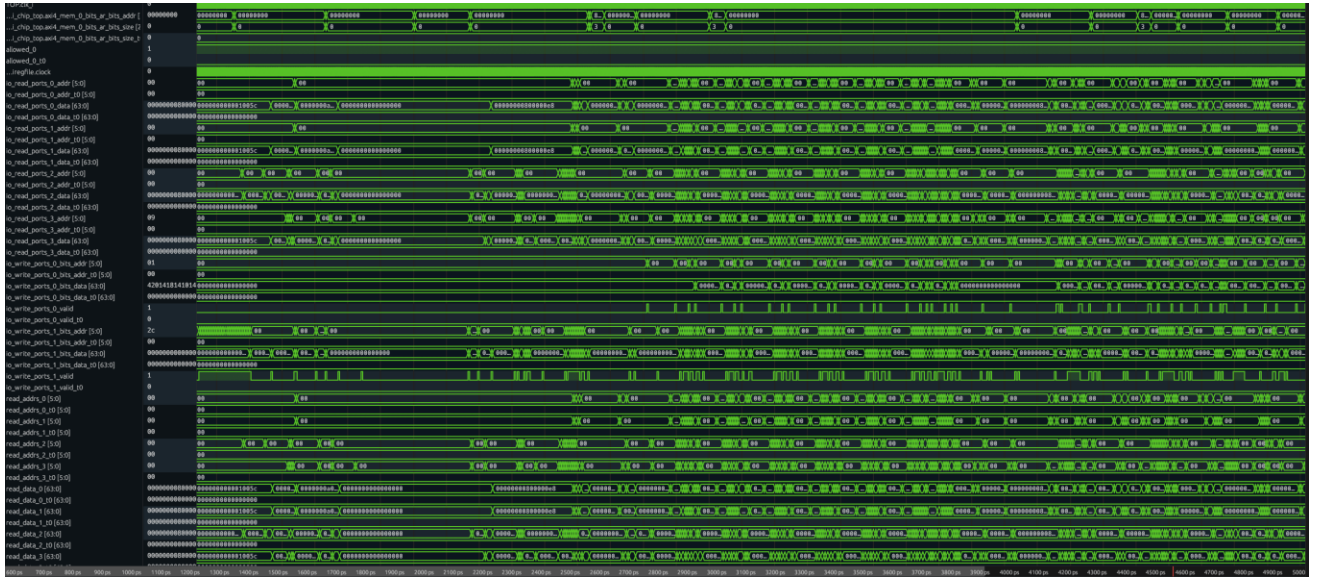
Scalable:
Graph generation in seconds - minutes

Results

BOOM – Spectre:
A speculative load leaves a trace in the cache
and leaks through the
Miss Status Holding Register (MSHR)



17 317 tainted signals

Pathfinder

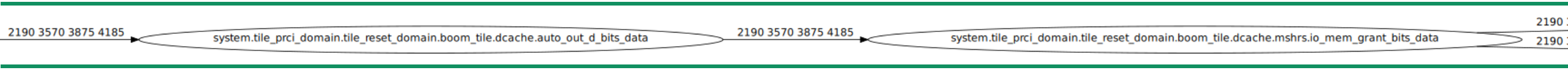
Taint Graph

213 nodes

...

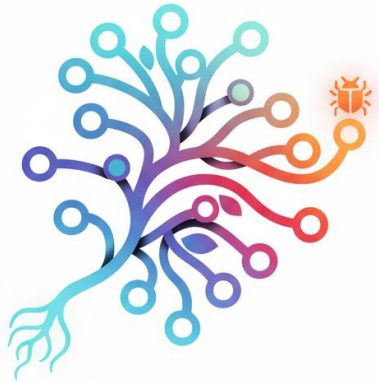
...

SPECTRE



Conclusion

- **Unified** taint tracking and self-composition



- Introduced **Pathfinder**
  - **Graphical aid** for **faster** information flow violation **debugging**
  - Reduces signals that need to be manually examined by **up to 700x**

Thank you! Questions?

Code:

comsec-group/pathfinder

Information:

https://comsec.ethz.ch/research/hardware-design-security/pathfinder/

Contact:

https://www.linkedin.com/in/katharina-ceesay-seitz-ba521087/

kceesay@ethz.ch, flavien.solt@eecs.berkeley.edu

References

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[2] L. Deutschmann et al., "A Scalable Formal Verification Methodology for Data-Oblivious Hardware", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems

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[4] M. Orenes-Vera et al., "AutoCC: Automatic Discovery of Covert Channels in Time-Shared Hardware", MICRO 2023

[5] Z. Wang, "Specification and Verification of Side-channel Security for Open-source Processors via Leakage Contracts", CCS 2023

[6] S. Dinesh, "H-Houdini: Scalable Invariant Learning", ASPLOS 2025

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[8] M. Tiwari et al., “Complete information flow tracking from the gates up,”, ASPLOS 2009

[9] A. Ardeshiricham, "Register transfer level information flow tracking for provably secure hardware design", DATE 2017

[10] F. Solt, B. Gras, K. Razavi, "CELLIFT: Leveraging Cells for Scalable and Precise Dynamic Information Flow Tracking in RTL", USENIX Security 2022

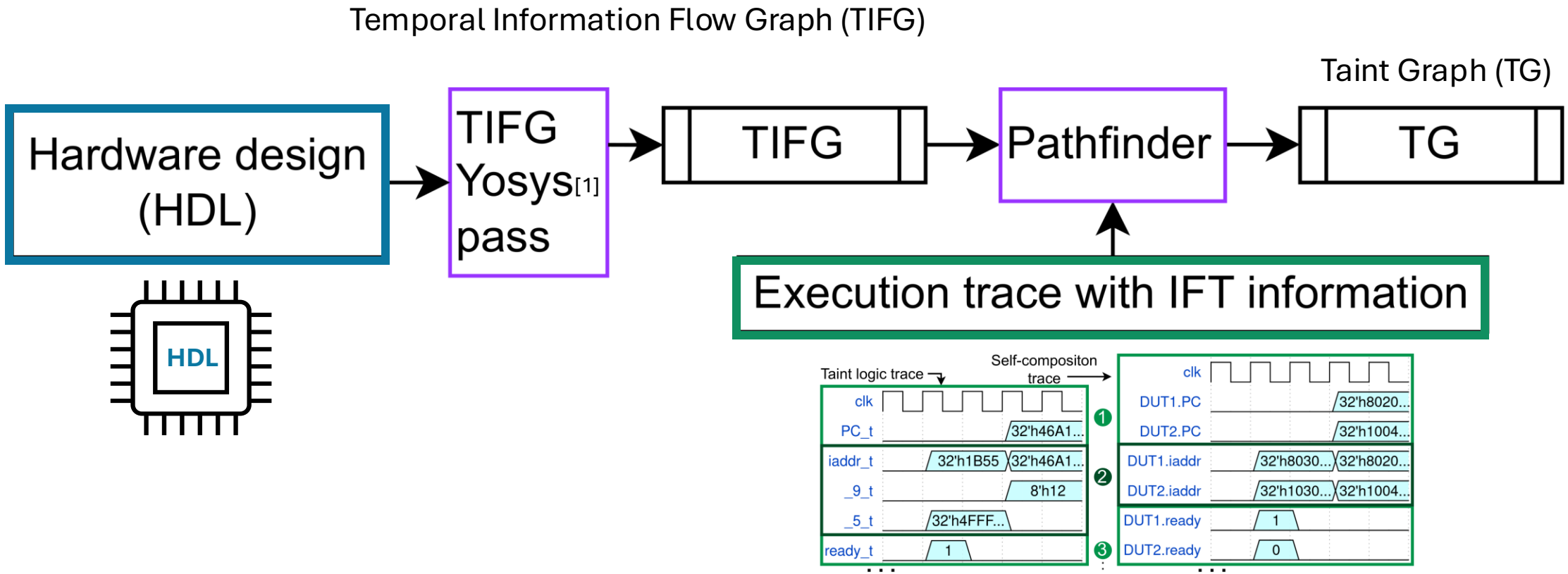
[11] Y. Hsiao et al., "RTL2MμPATH: Multi-μPATH Synthesis with Applications to Hardware Security Verification", MICRO 2024

[12] K. Ceesay-Seitz, F. Solt, K. Razavi, "μCFI: Formal Verification of Microarchitectural Control-flow Integrity", CCS 2024

[13] T. Kovats, F. Solt, K. Ceesay-Seitz, K. Razavi, "MileSan: Detecting Exploitable Microarchitectural Leakage via Differential Hardware-Software Taint Tracking", CCS 2025

BACKUP

Toolflow

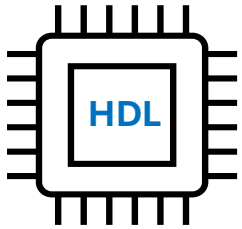


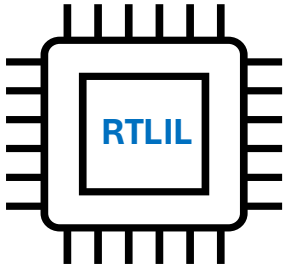
NEW

HDL = Hardware Description Language
IFT = Information Flow Tracking

[1] Yosys Open SYnthesis Suite - https://github.com/YosysHQ/yosys

CellIFT Yosys [1] pass

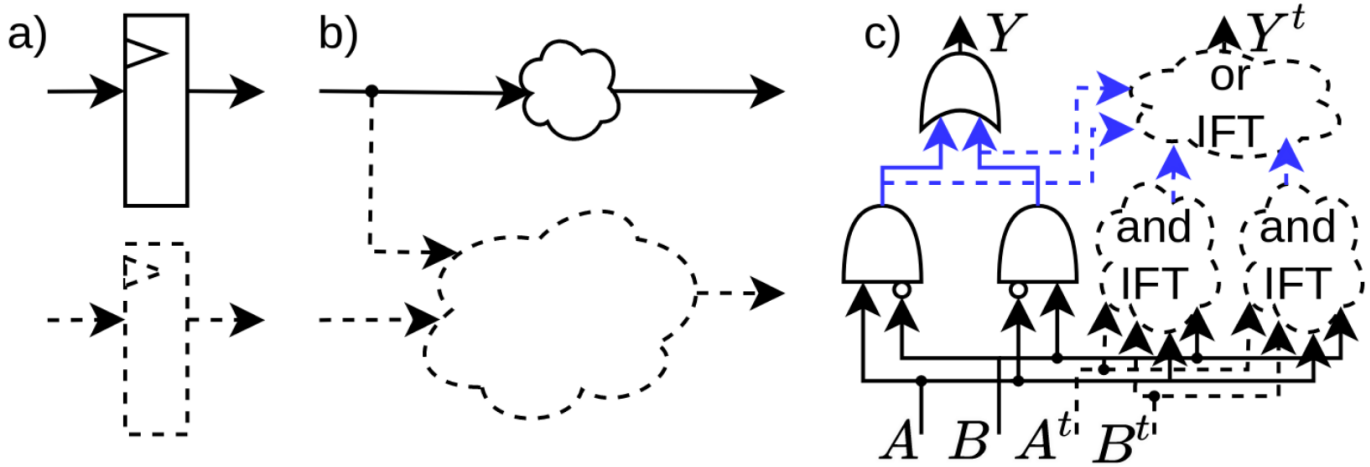


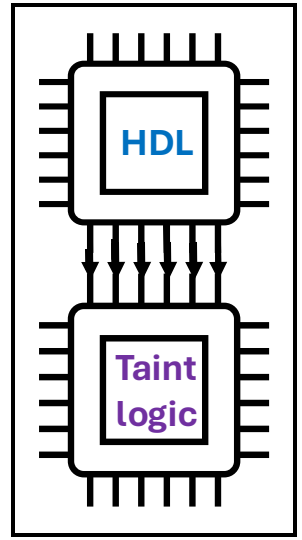


[2]

∀ cells (flip flops, logic cells, ...):

- Duplicate* in-/outputs for taint tracking
- Connect them with cell-type dependent taint tracking logic





a) State-holding cells
b) Combinational block
c) Gate-level output of Yosys

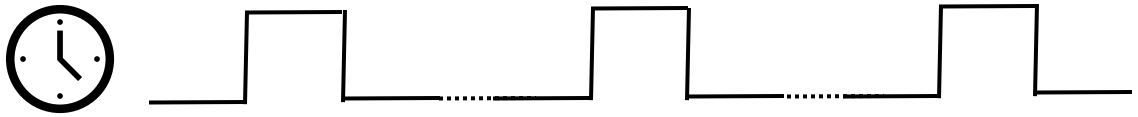
*it is possible to add multiple independent taint instrumentations. Each in-/output gets a taint representation per instrumentation.

[1] Yosys Open SYnthesis Suite - https://github.com/YosysHQ/yosys

[2] F. Solt, B. Gras, K. Razavi, "CELLIFT: Leveraging Cells for Scalable and Precise Dynamic Information Flow Tracking in RTL", USENIX Security 2022

µCFI - Microarchitectural Control-flow Integrity

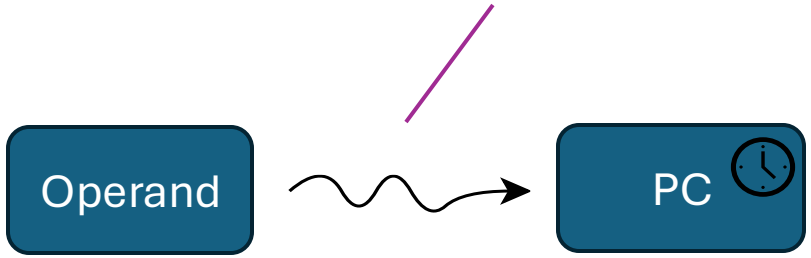
Microarchitectural control flow (µCF)



Program Counter (PC)

0x80000004 0x80000008 0x80001000

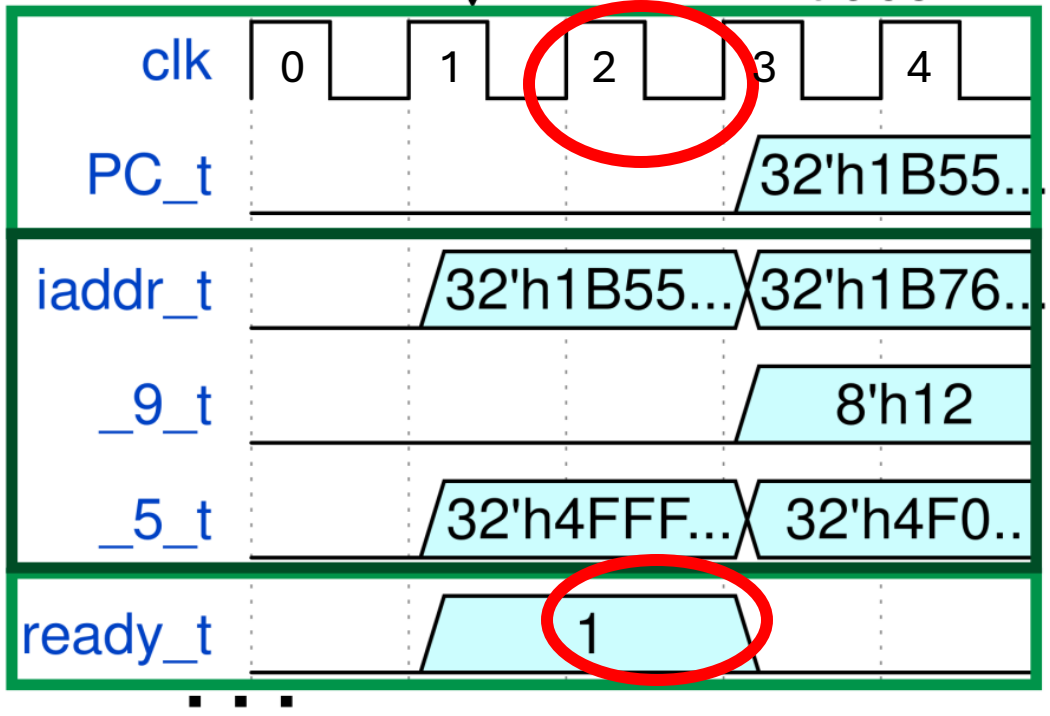
µCFI only allows explicitly ISA specified data dependencies of the µCF



K. Ceesay-Seitz, F. Solt, K. Razavi, "μCFI: Formal Verification of Microarchitectural Control-flow Integrity", CCS'24

ISA = Instruction Set Architecture

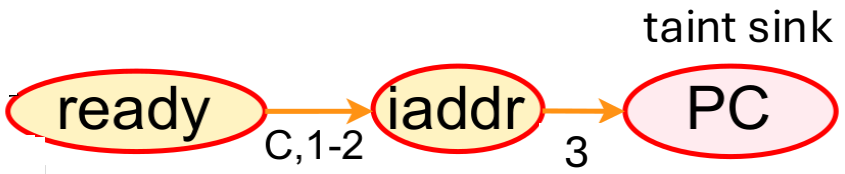
Pathfinder

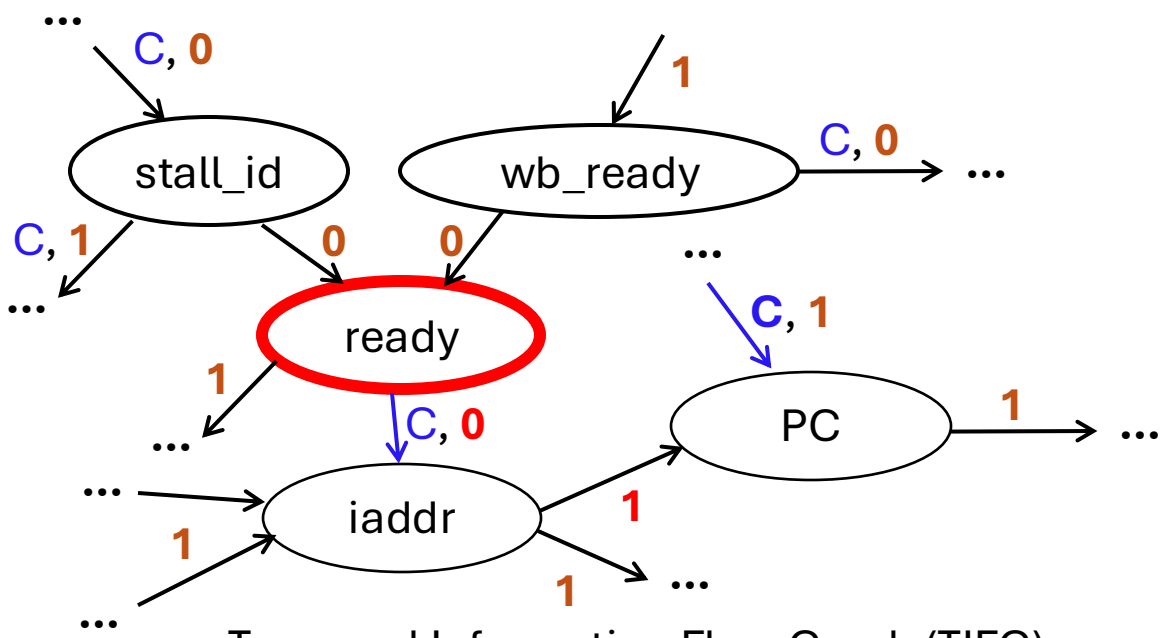


Taint Graph construction

Drivers with zero delay?

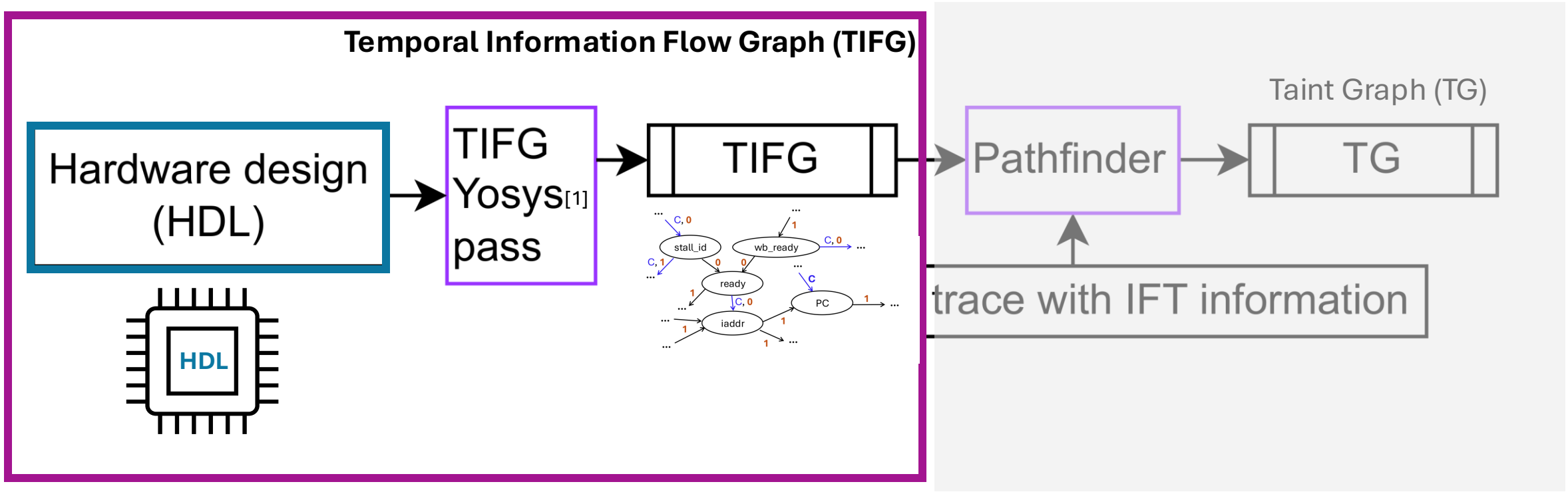
Yes.





Temporal Information Flow Graph (TIFG)

Toolflow



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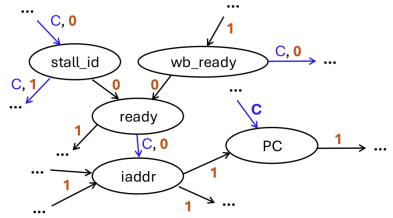
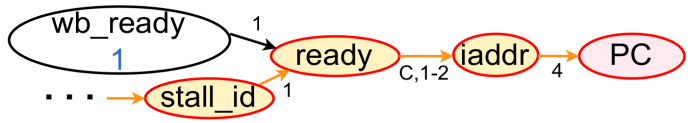
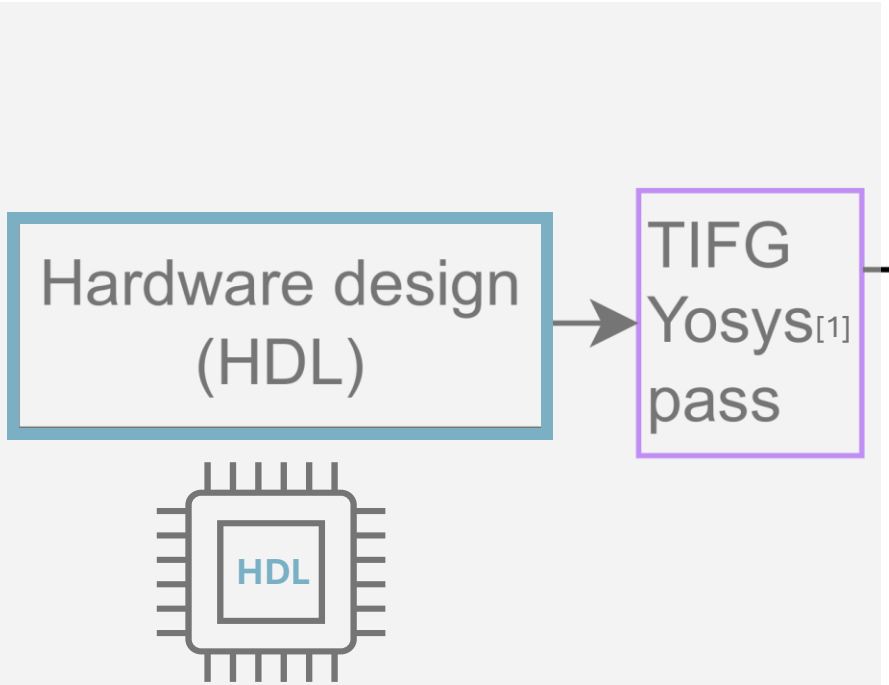
Toolflow

Temporal Information Flow Graph (TIFG)

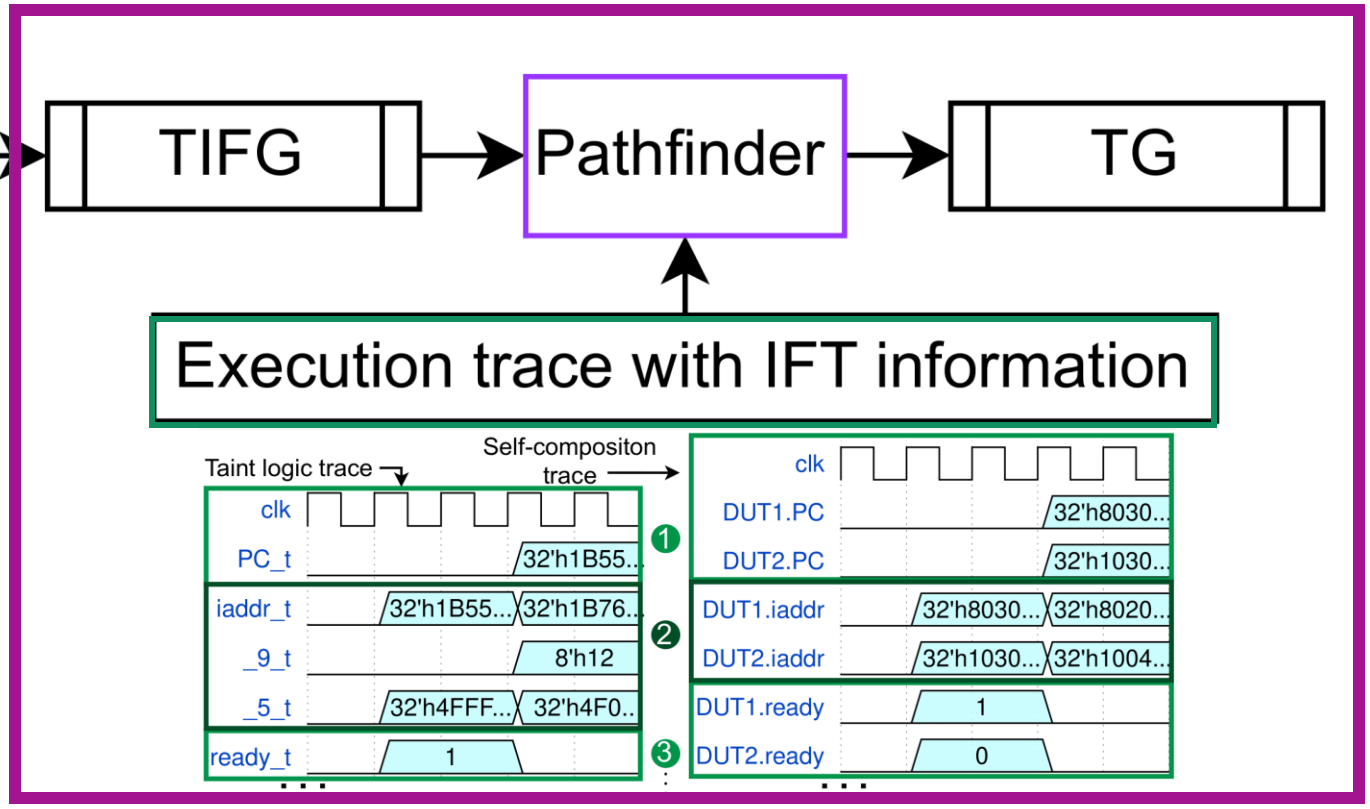


Taint Graph (TG)





TIFG Yosys[1] pass



NEW

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Unification: Pathfinder derives **taint** values from **differences** in self-composed design