Easy Formal With Jasper

Formal for Designers and Early Formal Verification

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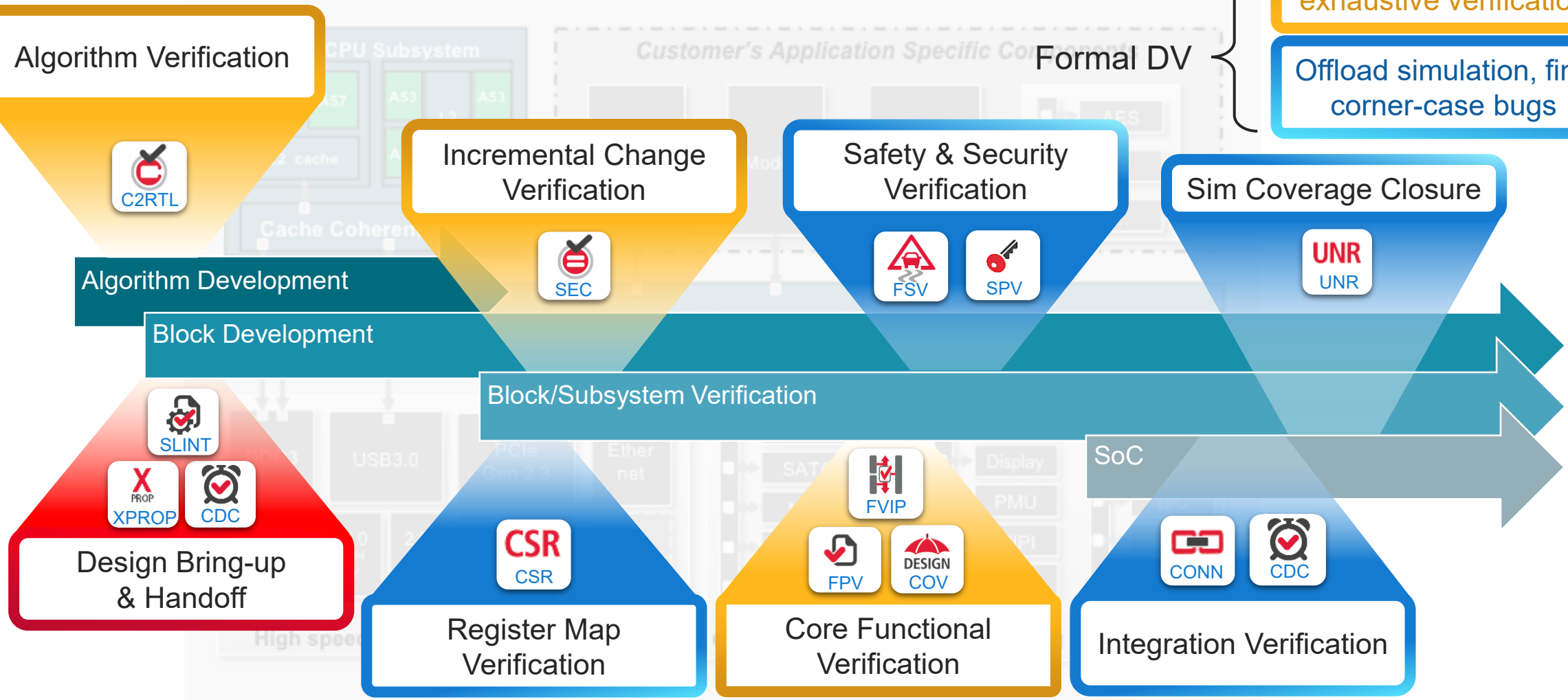
cadence®

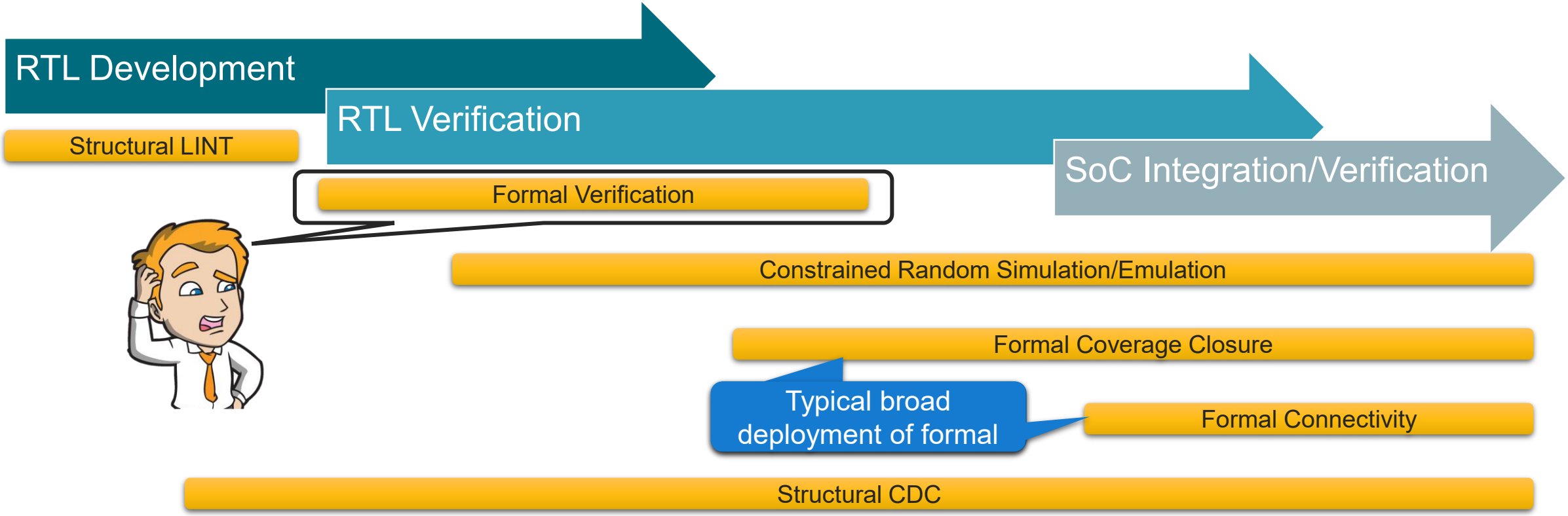
Breadth of Jasper Solutions Across Flow

Designers
- Handoff higher quality code earlier (shift left)
- Improve quality through exhaustive verification

Formal DV
- Offload simulation, find corner-case bugs



Design Verification Cycle



Challenge: Believe in the benefits of formal and want to deploy more but have limited or no expertise in house

Design Verification Cycle

- Broad set of high ROI use cases
- Highly automated → minimal expertise
- Early in DV cycle → maximum impact

Easy Formal w/ Jasper

RTL Development

RTL Verification

SoC Integration/Verification

Structural LINT

Implementation Checks

Formal Verification

Code Reachability
Overflow/Out-of-Bounds
FSM Deadlock
X Prop

Constrained Random Simulation/Emulation

Formal Coverage Closure

RTL Bringup

"Heartbeat" waveforms
Basic asserts

Typical broad deployment of formal

Formal Connectivity

Structural CDC

Functional CDC

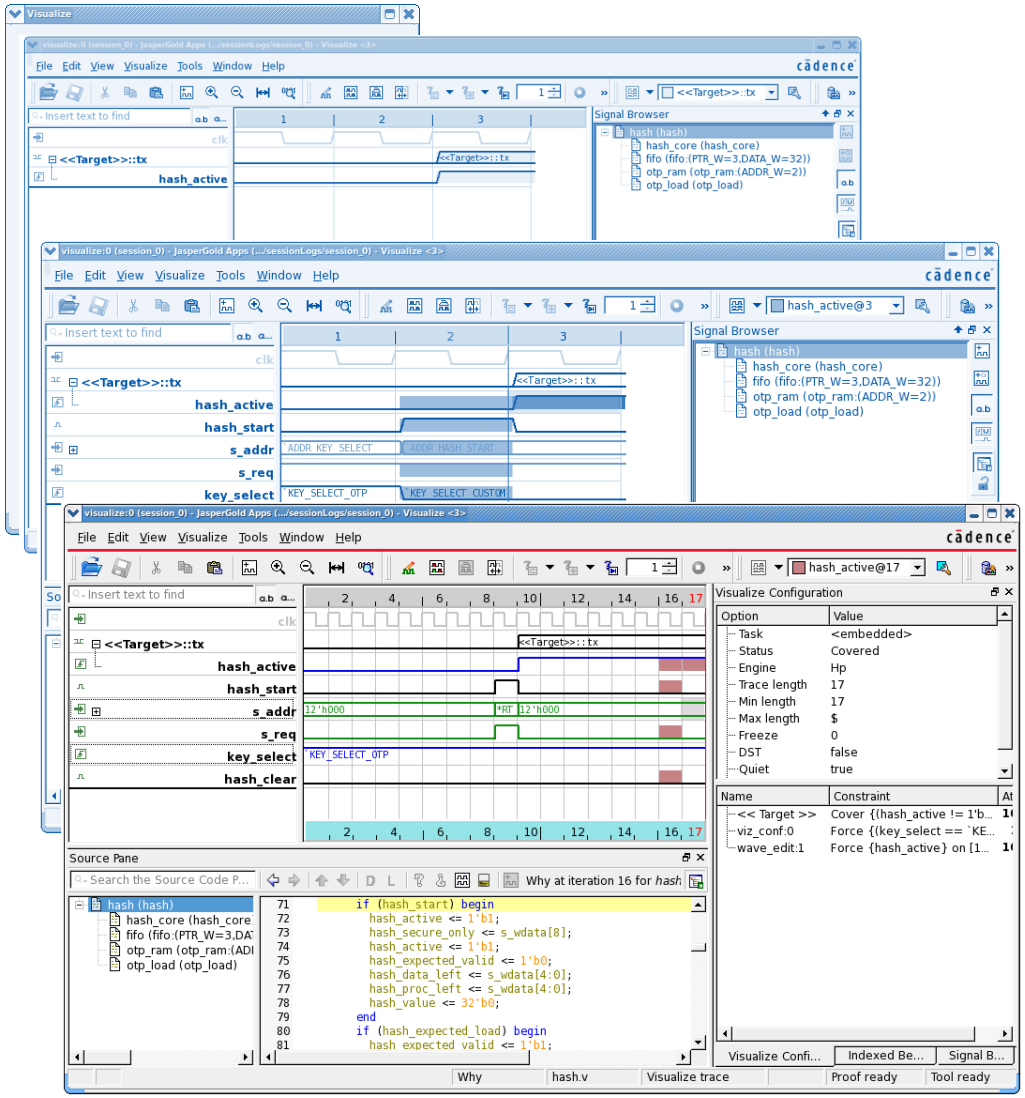
Protocol correctness

RTL Functional Equivalence (RTL == RTL'?)

Clock gating
Code refactoring
PPA optimizations

Start With Formal: Design Exploration

Design Exploration using the Visualize™ Environment



Create waveform:

- ✓ Specify target expression
- ✓ Formal engines create waveform

Understand waveform:

- ✓ Full signal visibility
- ✓ Integrated source code with value annotation
- ✓ **Why** feature takes you directly to relevant signals and code
- ✓ Highlight differences between waveforms

Change waveform:

- ✓ Change signal behavior with **WaveEdit** feature
- ✓ Extend waveform length
- ✓ Add constraints on-the-fly for **What-If** analysis
- ✓ Quiet down stimulus with **QuietTrace** feature

Low-Hanging Fruit: Auto-Formal Checks

Auto-Formal Checks Set 1

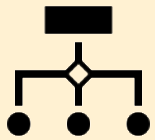
- RESET/INITIALIZATION CHECKS
  - All Flops initialized to a determined value
- AUTO_FORMAL_DEAD_CODE
  - RTL code block reachability
- AUTO_FORMAL_FSM_REACHABILITY
  - FSM state/transition reachability
- AUTO_FORMAL_SIGNALS
  - Signal Stuck-at
- AUTO_FORMAL_X_ASSIGNMENT
  - A reachable x-assignment was found
- AUTO_FORMAL_CASE
  - Default case reachability

Enabled with Jasper Superlint

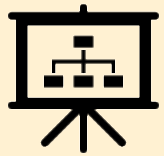
- Properties automatically generated by the tool
- Need no constraints
- Violation message view/property view for debug
- Full featured GUI and Resilient waivers
- Multi-Mode analysis NEW

Multimode Analysis

Many configs…



…one analysis



Run **multiple configs** and disposition violations in one **comprehensive view of all modes**. Compatible with all others next gen features.

Auto-Formal Checks Set 2 and 3

- Stage 1 Auto-Formal Checks +

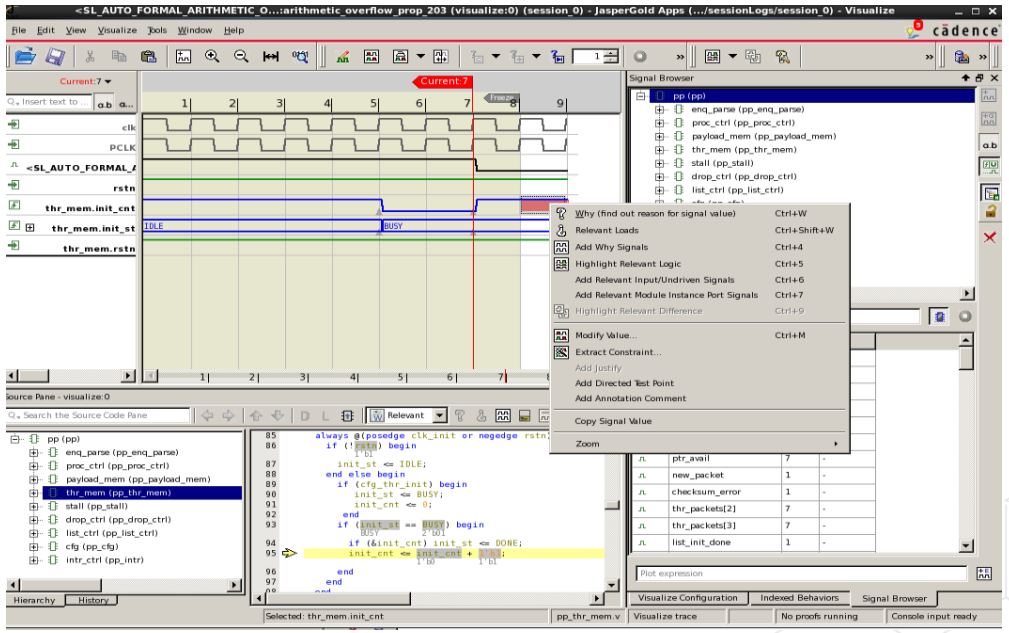
- AUTO_FORMAL_CASE
  - Priority/Unique violation
- AUTO_FORMAL_OUT_OF_BOUND_INDEXING
  - Index out of range
- AUTO_FORMAL_OVERFLOW
  - Overflow because of arithmetic operation, shift, Divide-by-zero, non-arithmetic
- AUTO_FORMAL_BUS
  - Bus Multiply driven, contention and floating
- AUTO_FORMAL_COMBO_LOOP
  - Combinational loop detection involving listed signals/wires/expressions
- AUTO_FORMAL_DEADLOCK_LIVELOCK
  - FSM state Deadlock/Livelock detection

Enabled with Jasper Superlint

SLINT

In addition to Stage 1

- Specify clocks/resets and some basic constraints
- FSM browser to debug FSM related failures
- Jasper Visualize to debug using waveforms

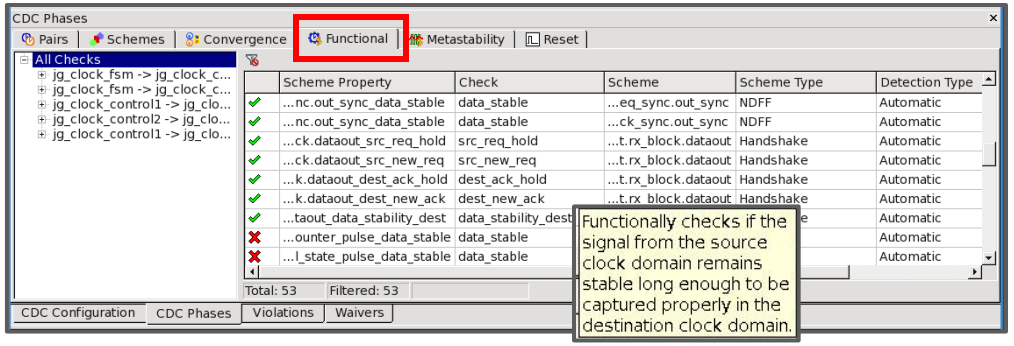


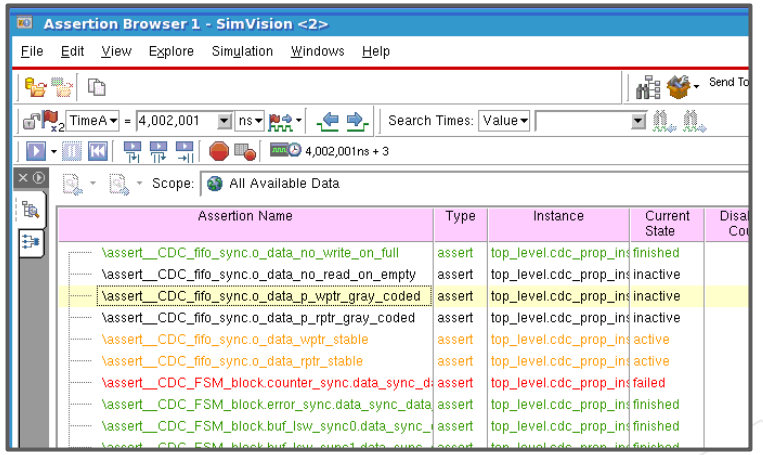
CDC Protocol Checks

Enabled with Jasper CDC

- CDC protocol checks
  - Auto-generated protocol checks for all identified synchronizers
  - Supports user-defined protocol checks for custom synchronizers
  - Requires very strong formal tool capabilities
    - Best in class Jasper formal engines
  - Export protocol checks to run in simulation

Protocol Checks	Synchronization Schemes
Control Path Stability	NDFF, NDFF_BUS, Pulse, Edge, Glitch Protector
Data Path Stability	MUX_NDFF, MUX_PULSE, Sync Enabler, Glitch Protector
Pulse Width Toggle Circuit	Pulse
Req/Ack Stability Data Stability Handshake Protocol	Handshake Synchronizer
Rear/Write Pointer Stability Overrun/Underrun Gray Encoding of Pointers	FIFO Synchronizer

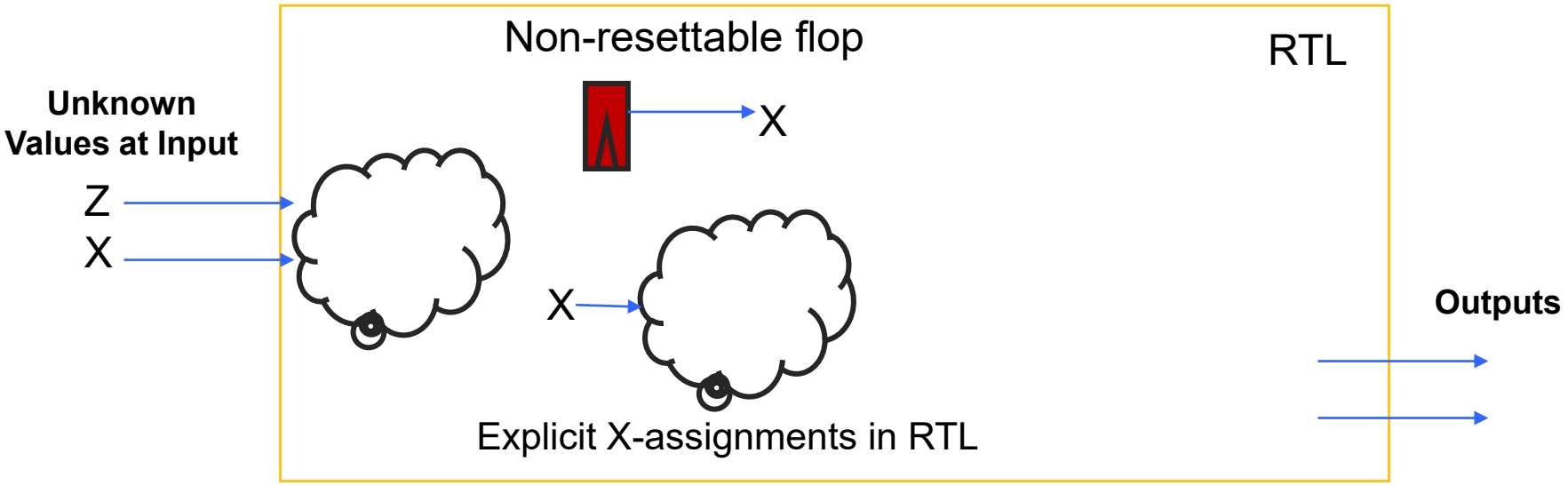


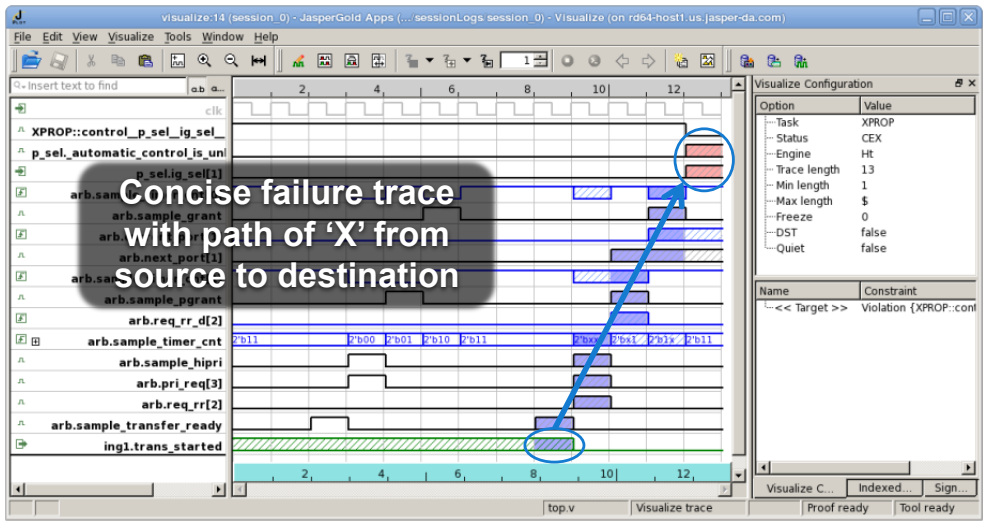


Worried About Xs?

Auto-X Checks

Enabled with Jasper XPROP

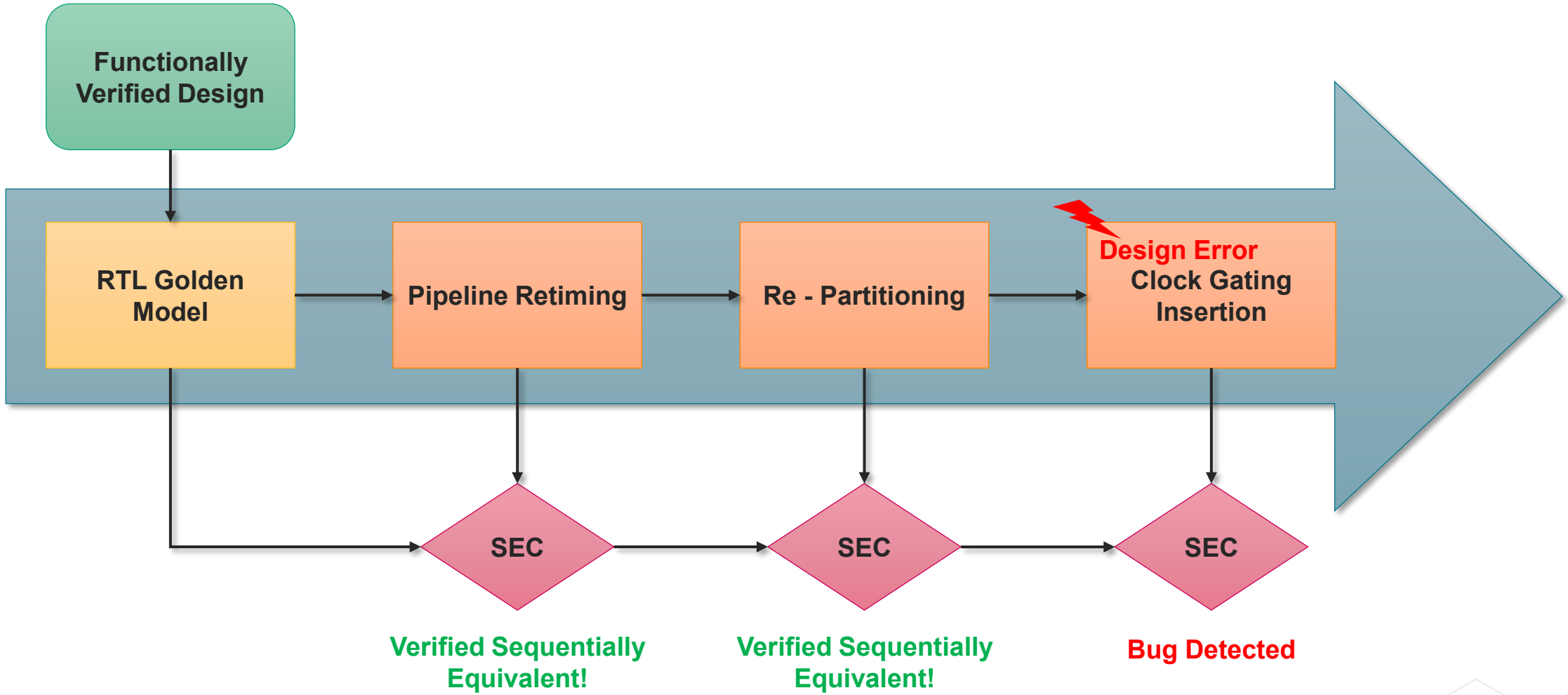




Changing RTL For PPA Optimizations?

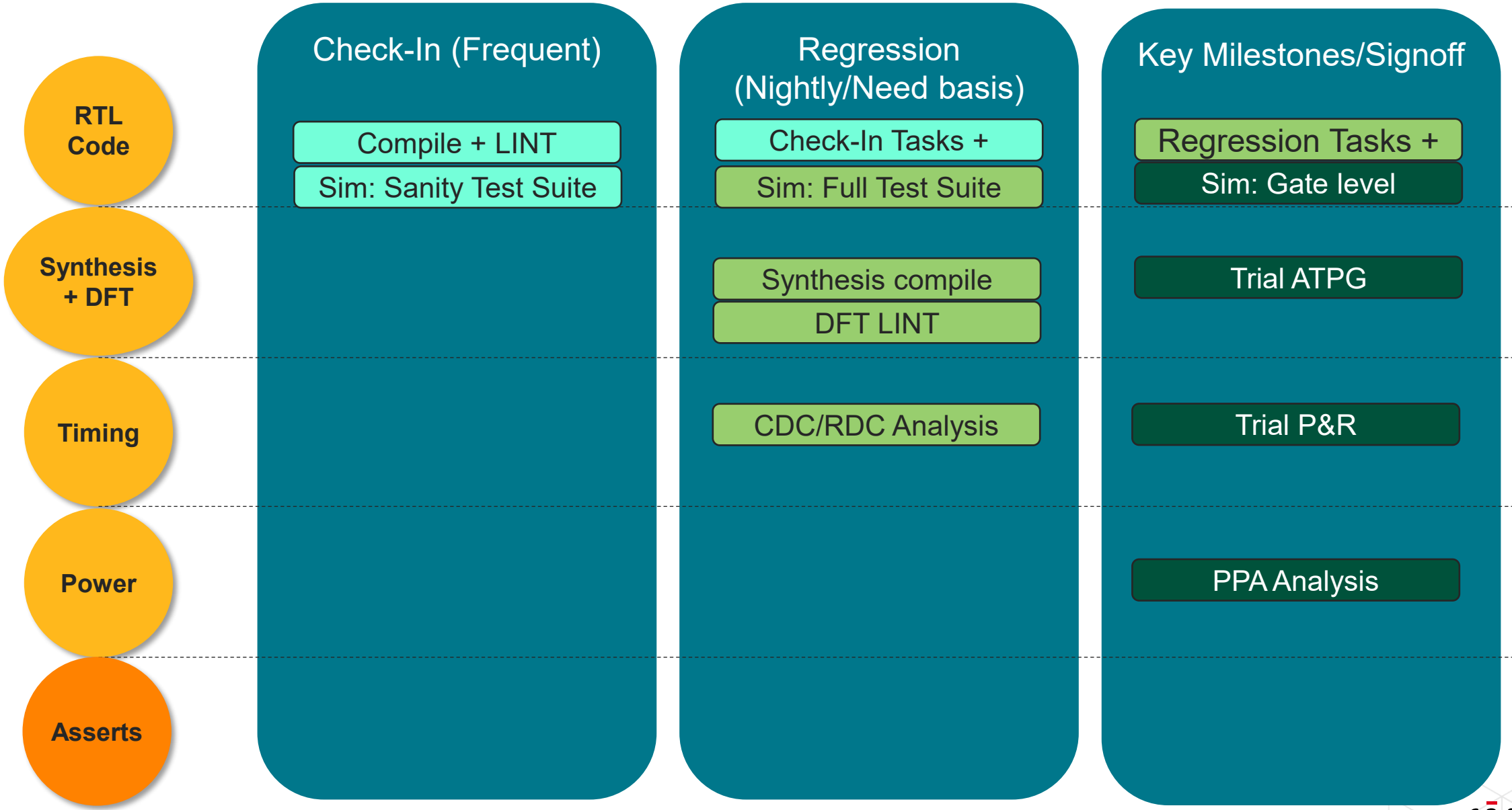
Check Functional Equivalence After Each Change

Enabled with Jasper SEC



Bringing it All Together

The Intersection: Designer/Early DV Tasks in Context of Timeframes



Augmented Task Map

Formal Enabled

RTL Code

Synthesis + DFT

Timing

Power

Asserts

Check-In (Frequent)

- Compile + LINT
- Sim: Sanity Test Suite
- Auto Formal Set 1 — SLINT

Regression (Nightly/Need basis)

- Check-In Tasks +
- Sim: Full Test Suite
- Auto Formal Set 2, 3 — SLINT
- Synthesis compile
- DFT LINT
- CDC/RDC Analysis
- CDC Auto-Checks — CDC
- Auto-X Checks — XPROP

Key Milestones/Signoff

- Regression Tasks +
- Sim: Gate level
- Trial ATPG
- Trial P&R
- PPA Analysis
- Clock Gating — SEC