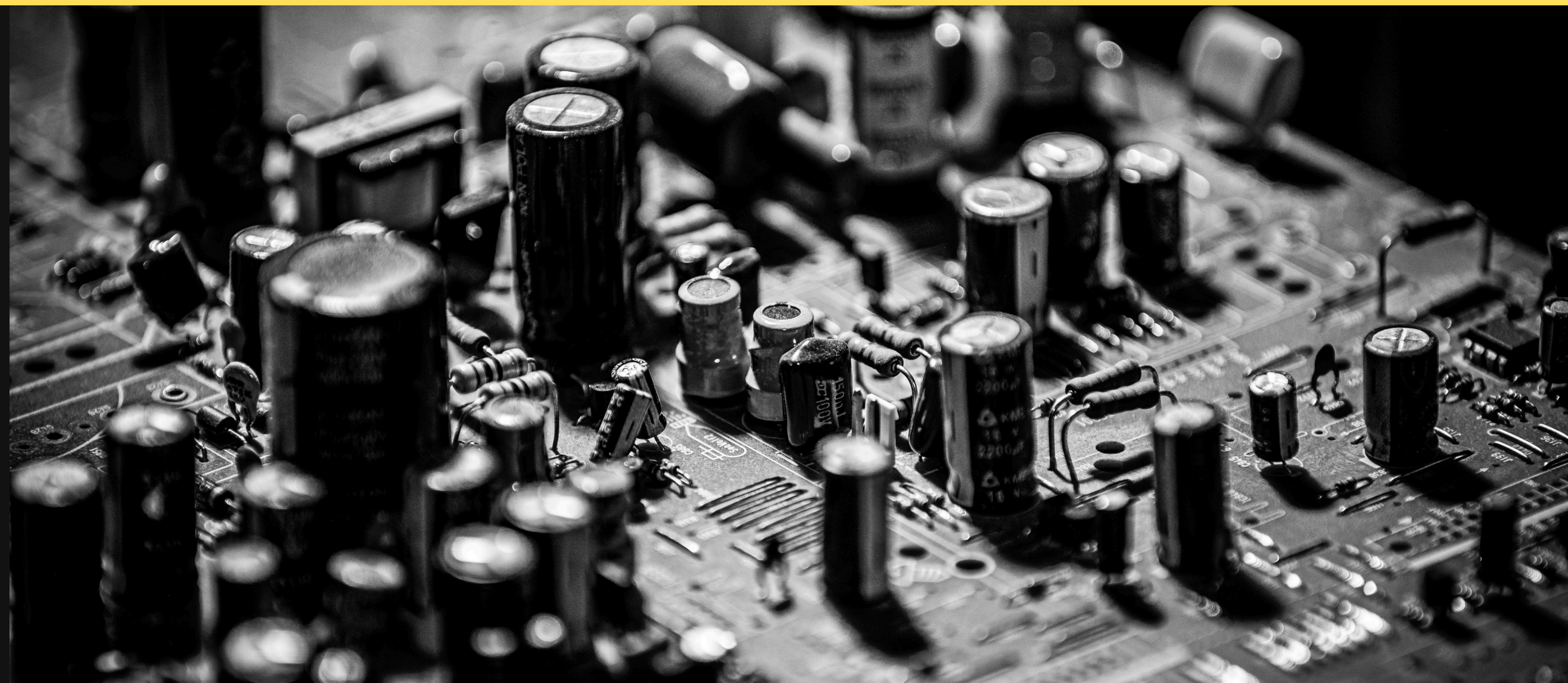
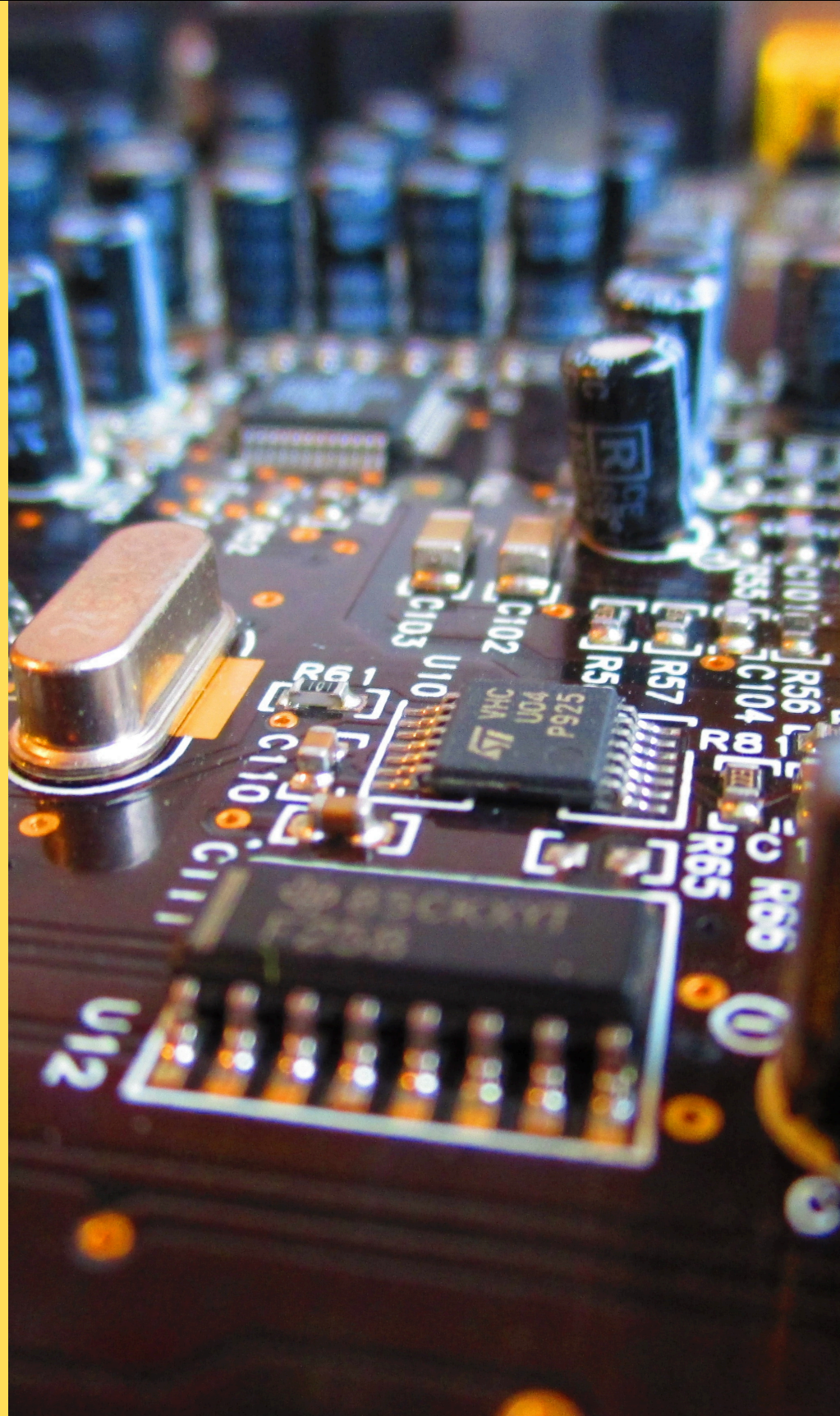


HIGH-SPEED CHALLENGES

CHALLENGES IN HIGH-SPEED DESIGN AND VERIFICATION (PCIe, UCIE, CXL)

Overview, Challenges,
and more





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INDUSTRY OVERVIEW

THE GROWING COMPLEXITY OF HIGH-SPEED INTERCONNECTS

Modern interconnect standards like PCIe, UCIe, and CXL are driving the next wave of high-performance computing. As data rates exceed tens of gigabits per second, maintaining signal integrity, power efficiency, and interoperability across complex multi-die architectures has become a major design challenge. The industry is increasingly relying on advanced simulation, modeling, and verification tools to ensure compliance, optimize channel performance, and meet the stringent timing and jitter requirements of high-speed interfaces.

BARRIERS TO EFFICIENCY AND INNOVATION

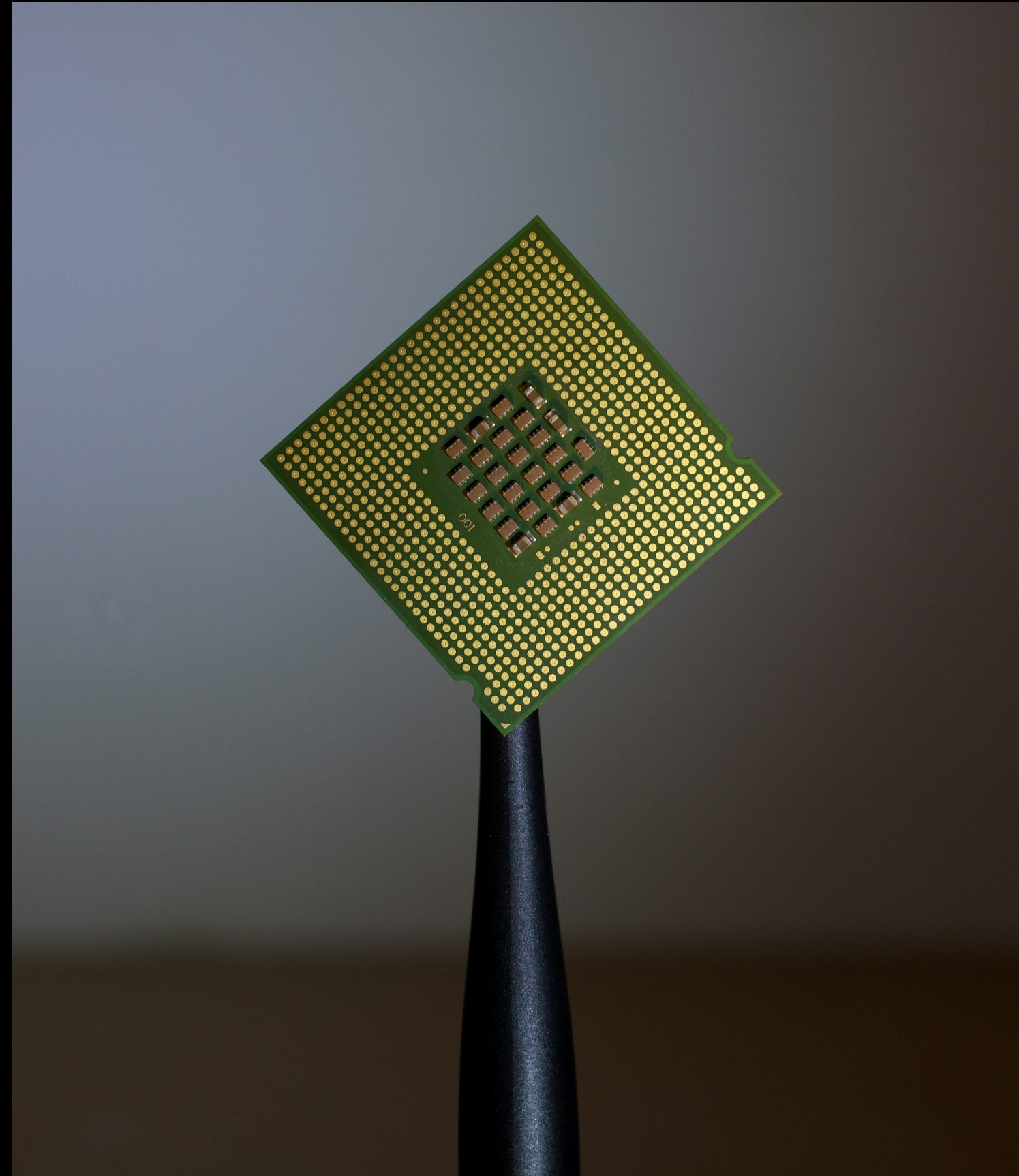
Design Complexity

Managing high-frequency clocks, wide data paths, and multi-TLP logic drastically increases timing closure effort.

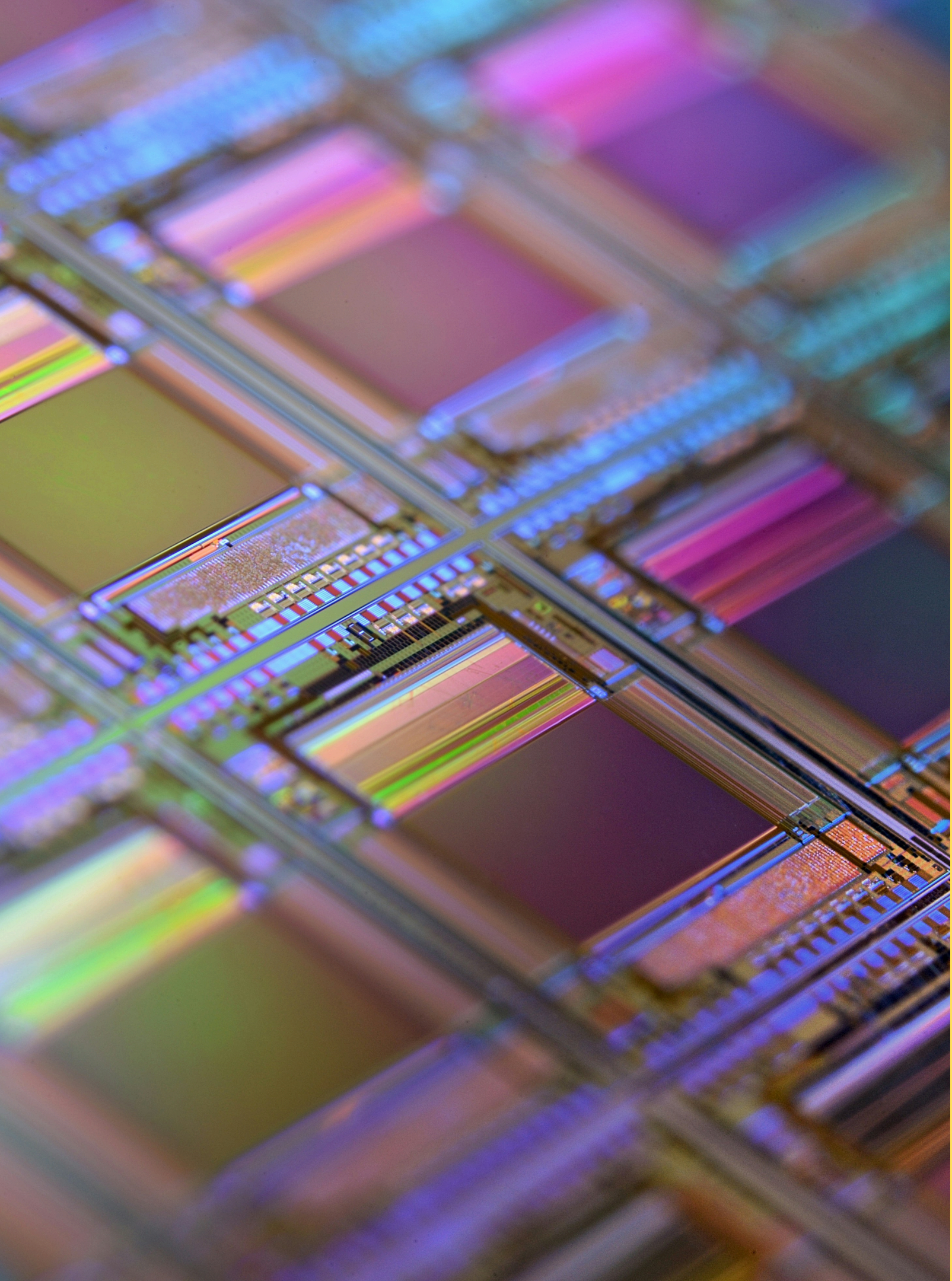
Verification Explosion

Tens of thousands of test configurations demand scalable, automated verification across diverse interface and power modes.

CORE STRUGGLES



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CHALLENGES

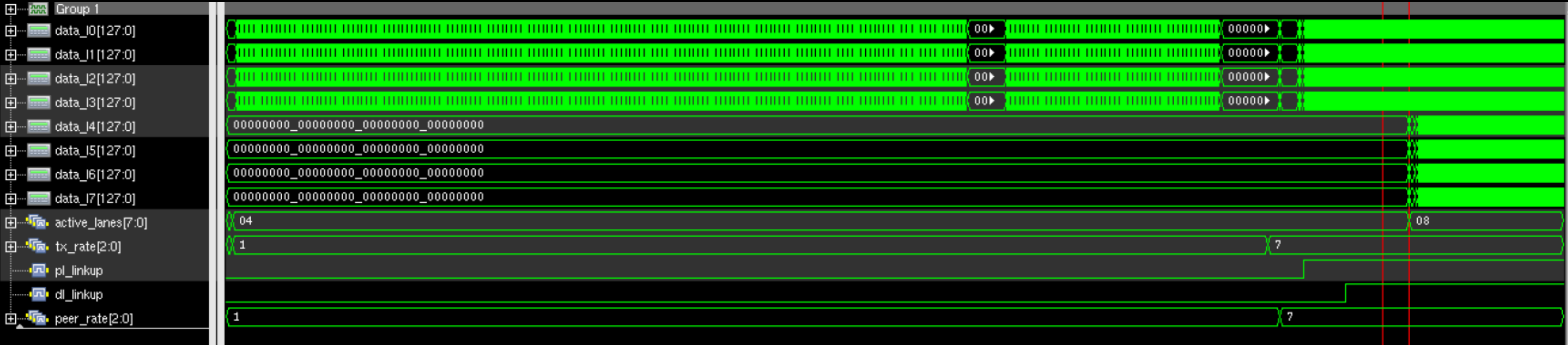
- High frequency clocks and multi million gates
- Wider internal databus architectures
- Multi TLP Handling
- Start/End TLP Positions
- Multiple interface widths on Application and PHY
- PCS Handling at Digital
- Complex Spec concept Handling like Flit Alignments, Flit to non Flit conversions and vice versa, Low power domain architectures, IDE, Dynamic Upsize/Downsize of lanes
- Getting Enumerated
- Each testcase – 40+ Configurations: All put together 10000+ Testcases for each IP/Subsystem
- Backward compatibility verification Checks
- Configurable/ Leveragable/ Plug-and-Play Modules architected in both Design and Verification



DOWNSIZE

Signal	Value	Unit	Value	Unit
pclk				
\data_0[127:0] [127:0]	00000000_00000000_00000000_00000000			
\data_1[127:0] [127:0]	00000000_00000000_00000000_00000000			
\data_2[127:0] [127:0]				
\data_3[127:0] [127:0]				
\data_4[127:0] [127:0]				
\data_5[127:0] [127:0]				
\data_6[127:0] [127:0]				
\data_7[127:0] [127:0]				
\data_8[127:0] [127:0]			00000000_00000000_00000000_00000000	
\data_9[127:0] [127:0]			00000000_00000000_00000000_00000000	
\data_10[127:0] [127:0]			00000000_00000000_00000000_00000000	
\data_11[127:0] [127:0]			00000000_00000000_00000000_00000000	
\data_12[127:0] [127:0]			00000000_00000000_00000000_00000000	
\data_13[127:0] [127:0]			00000000_00000000_00000000_00000000	
\data_14[127:0] [127:0]			00000000_00000000_00000000_00000000	
\data_15[127:0] [127:0]			00000000_00000000_00000000_00000000	
active_lanes[7:0]	16		8	
tx_rate[2:0]	6			

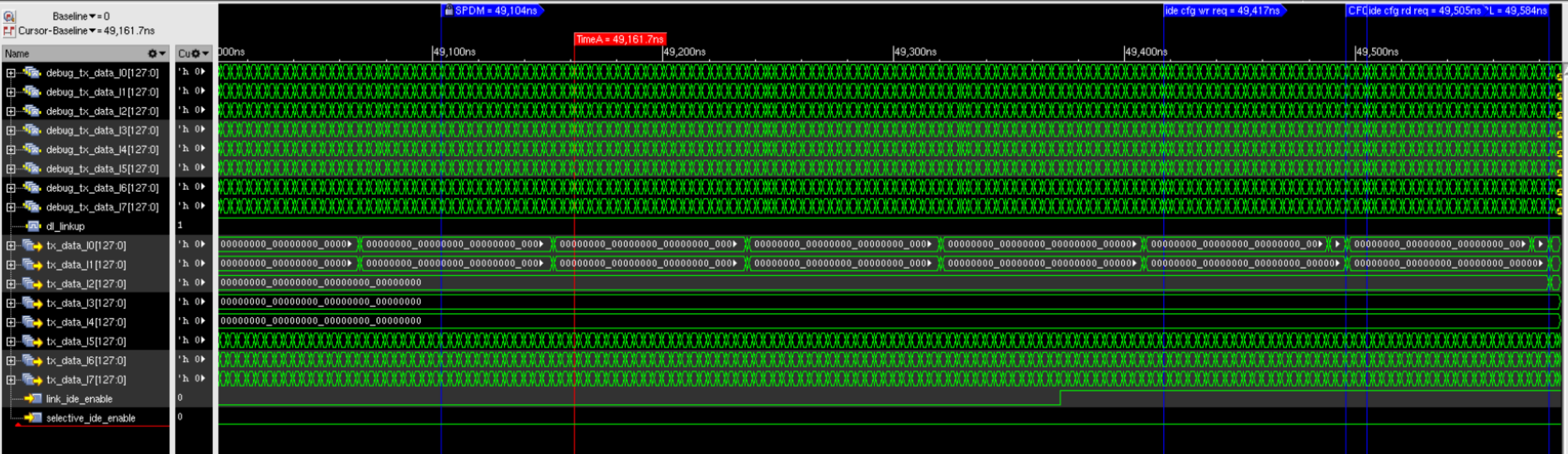
UPSIZE



CXL FLIT ALIGNMENT



IDE

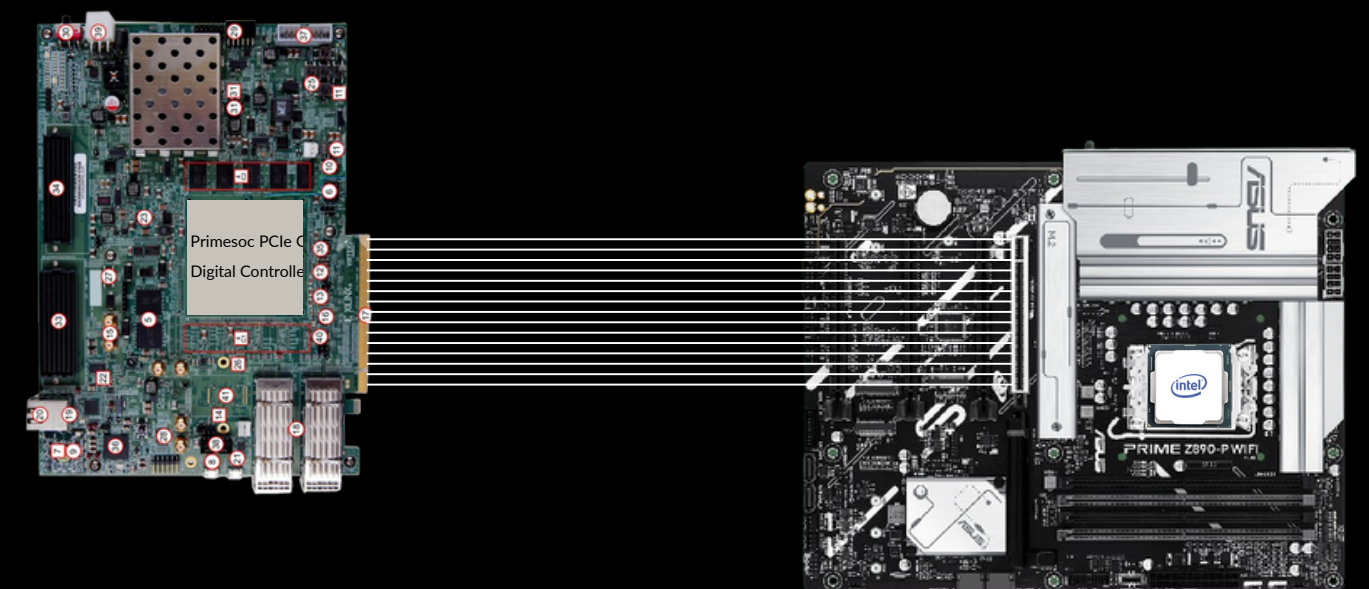


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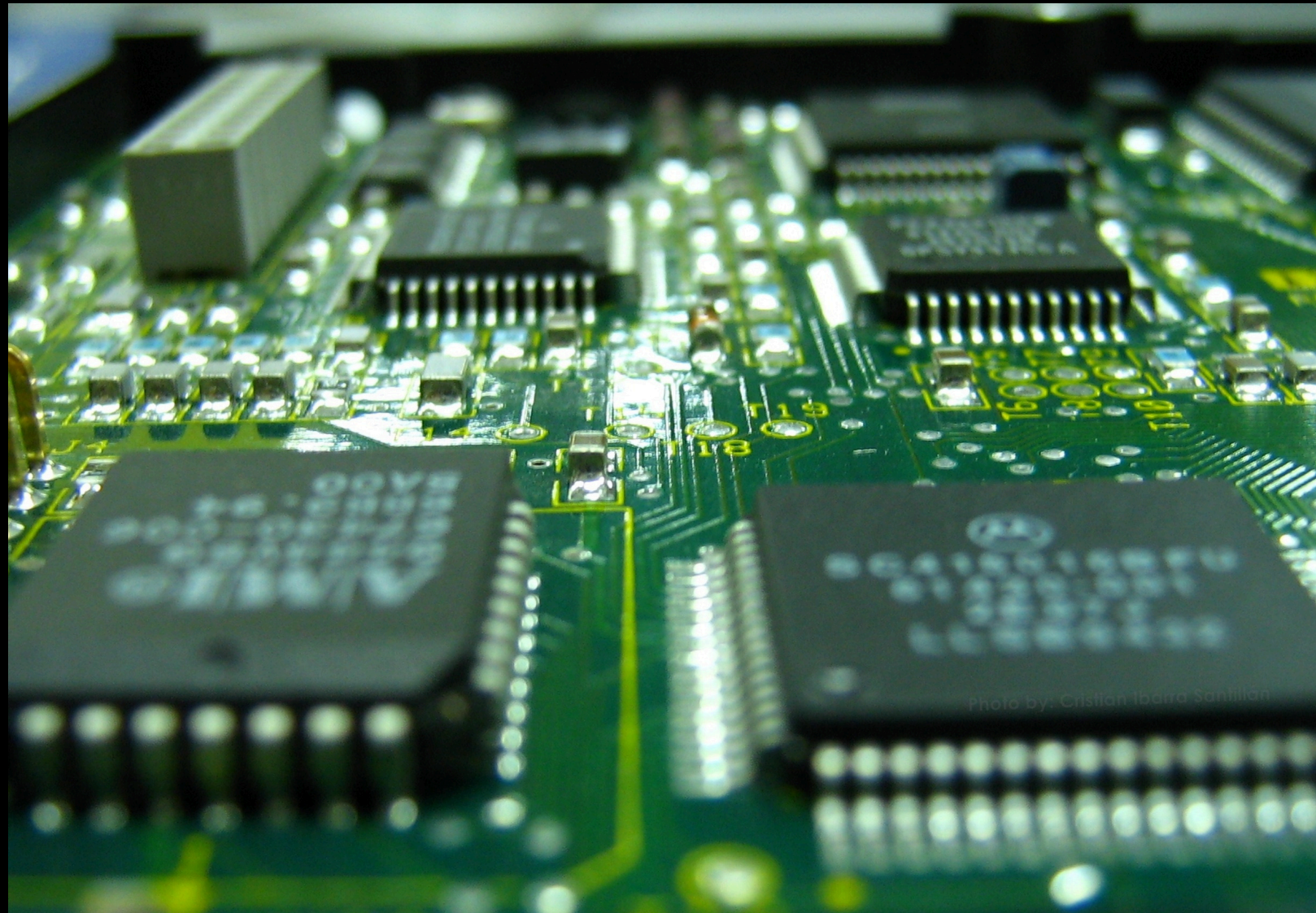
ENUMERATION DETAILS

```
010000-0xfe010fff]
e 00 class 0x010802 PCIe Endpoint
100000-0x8d103fff 64bit]
bus 01]
e 00 class 0x000580 PCIe Endpoint
000000-0x8d000fff]
ed Tags
lable PCIe bandwidth, limited by 16.0 GT/s PCIe x1 link at 0000:00:06.0 (capable of 64.000 Gb/s with 64.0 GT/s PCIe x1
bus 02]
```

PCIe Gen 6 (64GT/s) downgraded to PCIe Gen 4 (16 GT/s)



THANK YOU



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