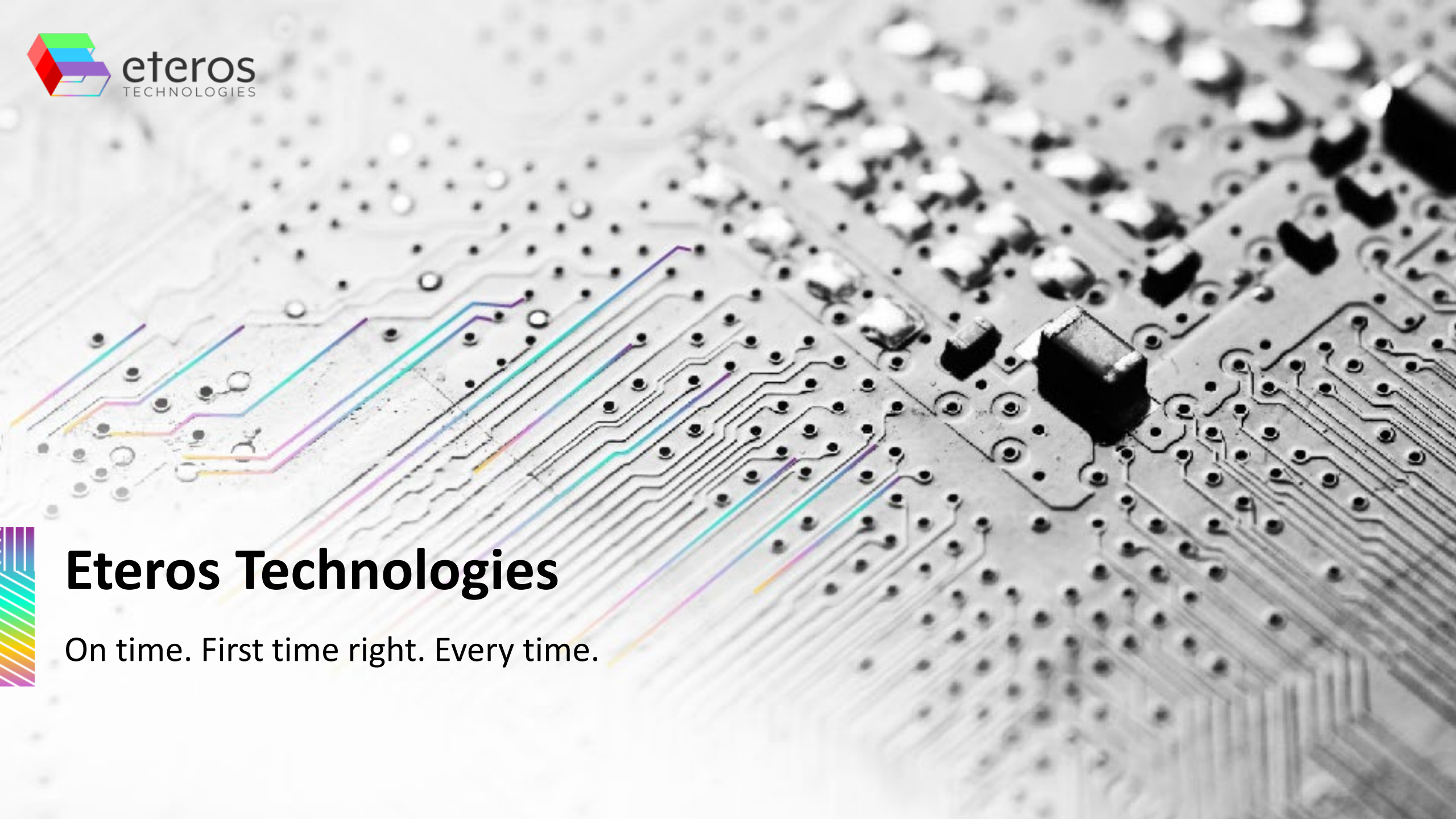
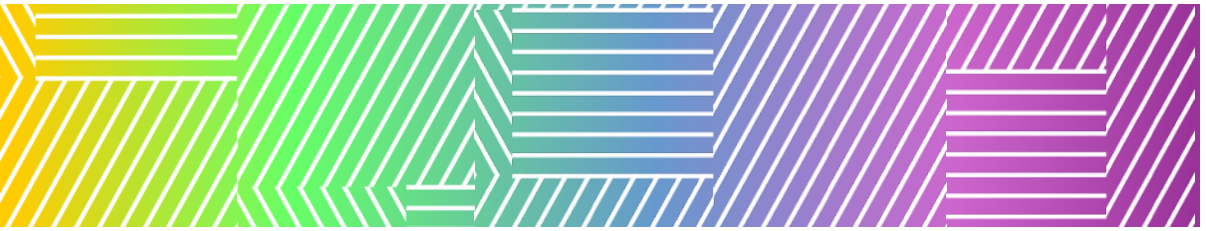


Eteros Technologies

On time. First time right. Every time.



A Quick Introduction

Who We Are

- 4.5 year-old company
- 130+ years combined leadership experience
- Provider of quality end-to-end semiconductor engineering services
- Experts in Automotive, AI & Datacenter SoCs
- Growth track record built on our compelling promise

On time. First time right. Every time.

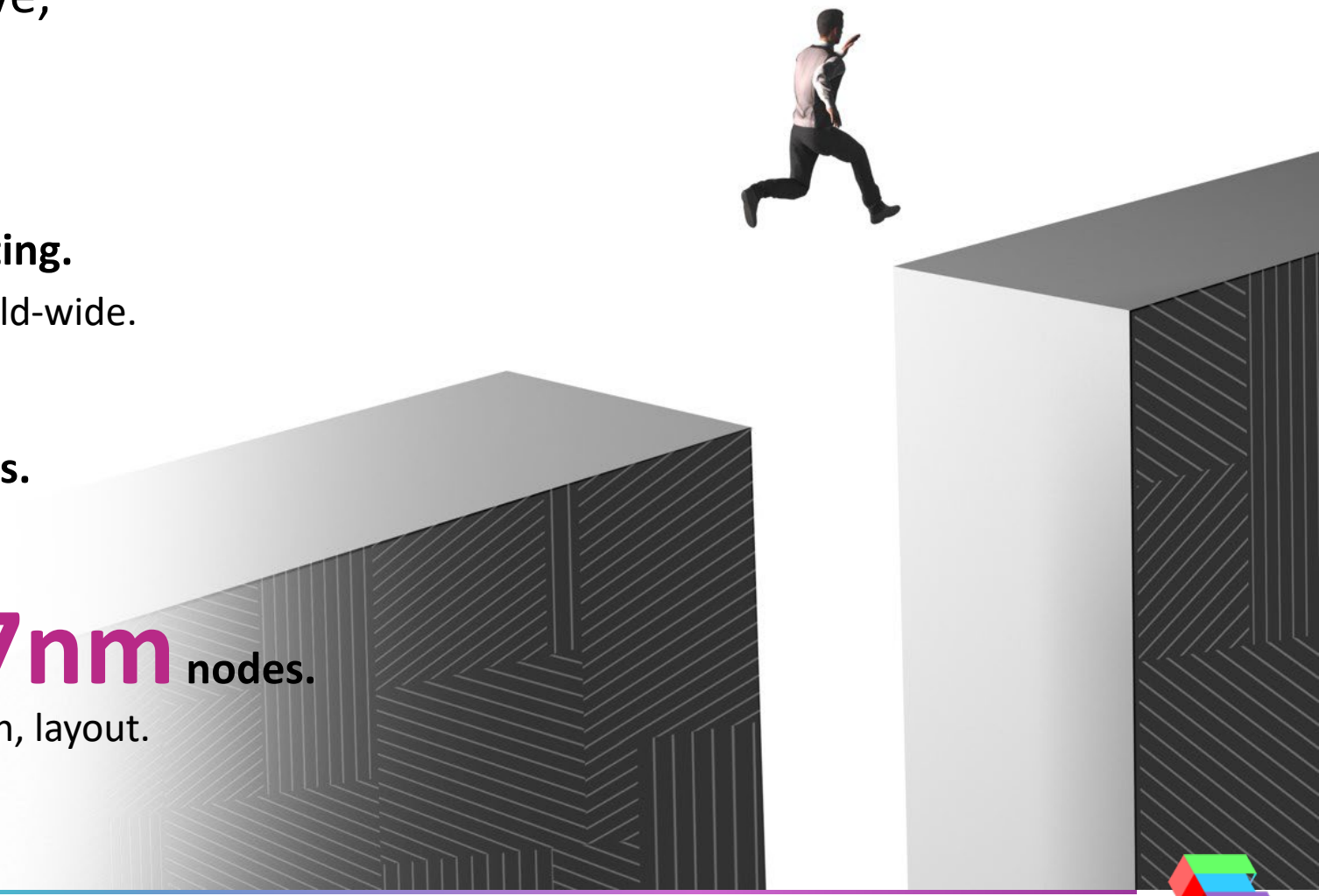
Why Talk to Us?

Proven track record in Automotive,
AI & Datacenter SoCs

25 **customers and counting.**
From startups to large caps world-wide.

16+ **tape-outs in 4 years.**

3nm, 5nm, 7nm **nodes.**
Netlist to GDS, DFT, analog design, layout.



Why Talk To Us?

Customer-centric model for on-time, on-cost delivery

Right expertise + right sized team
+ streamlined program management.
To solve any customer problem.

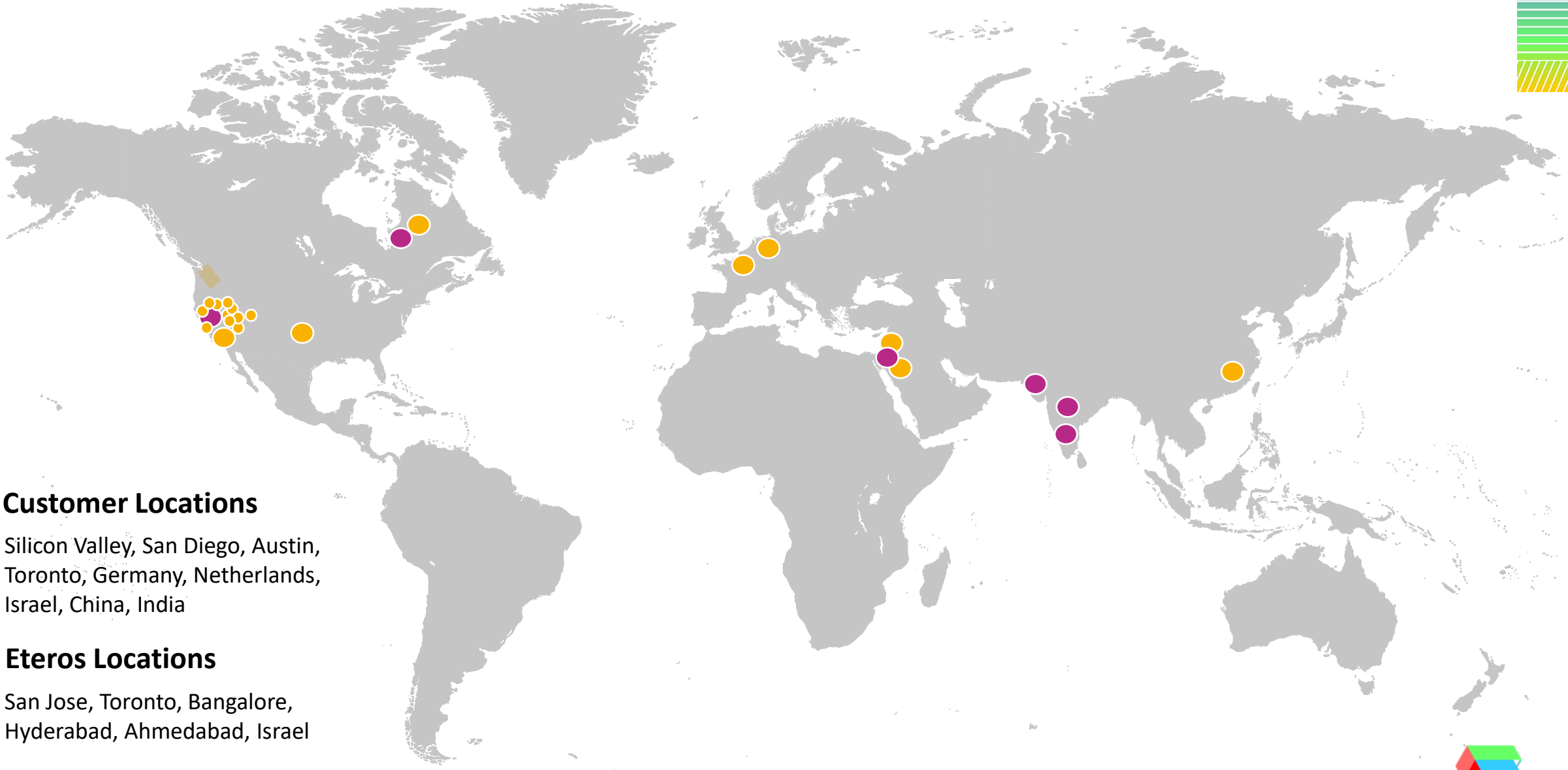
145+ engineers deployed globally.

On Time. First time right. Every time.

Steady Growth Over 4 Years

	2020	2021	2022	2023	2025 YTD	
Expanding Customer Portfolio	2	8	18	21	25	Across Automotive, AI, Datacenter & other verticals.
Deepening Customer Engagement						Augmentation -> turnkey/ODC Increasing headcount per customer.
Growing Team	5	20	40+	80+	145+	In-house team + worldwide talent pool.

Global Footprint for Nearshore Support



- **Customer Locations**

  Silicon Valley, San Diego, Austin, Toronto, Germany, Netherlands, Israel, China, India

- **Eteros Locations**

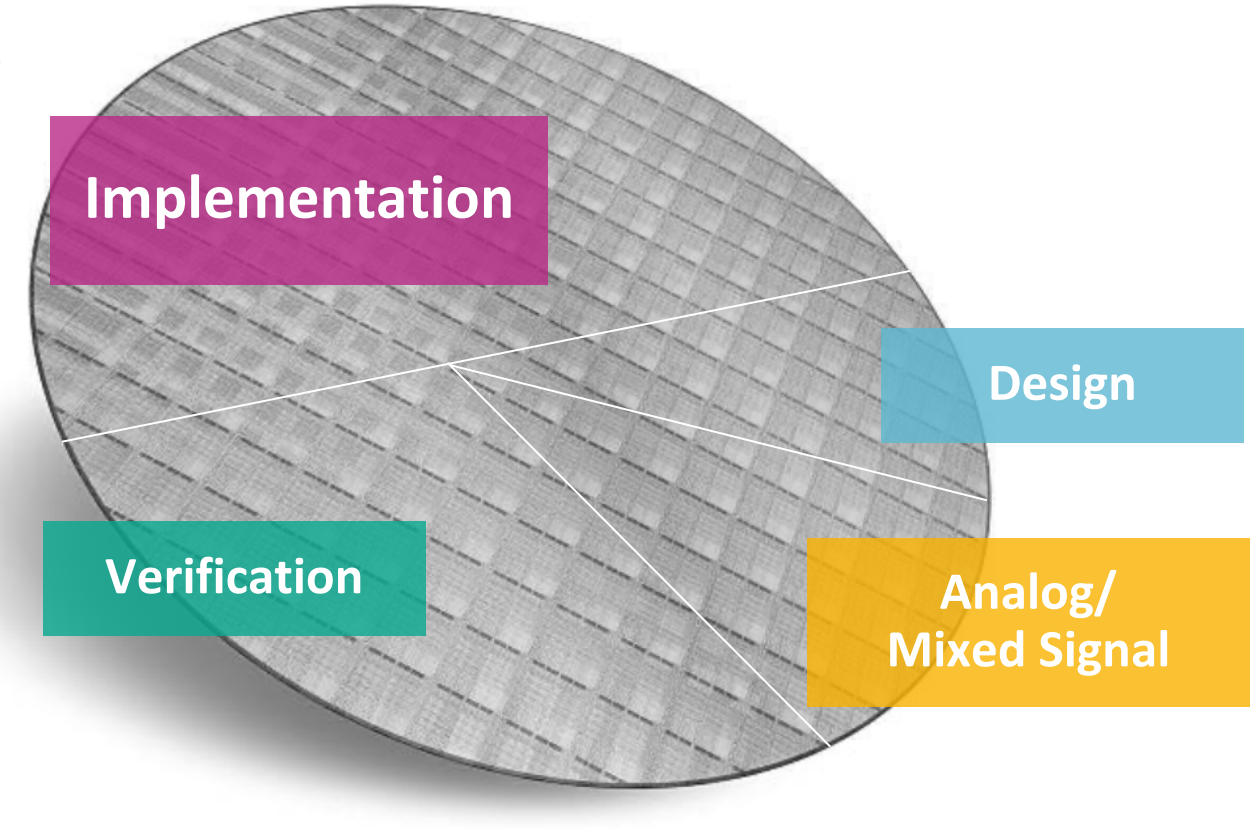
  San Jose, Toronto, Bangalore, Hyderabad, Ahmedabad, Israel

What We Do

End-to-End Silicon Design Services

- Flow & Methodology Dev
- Netlist -> GDS
- Constraints Development
- DFT & Post-Silicon Debug
- Physical verification
- Sign-off

- IP Verification: PCIe, USB, MIPI, DDR, ARM CPU & BUS protocols
- Subsystem Verification
- SoC
- SV/UVM



- RTL
- Foundation IP
- Custom Std. Cell Dev & Char

- DACs/ADCs/PLL
- Power Management
- High Speed Serdes
- IP Porting
- Custom Layout

Business Models Tailored to Your Needs

Turnkey Project Execution

- SoW driven • On customer network with customer tooling OR @ Eteros
- Streamlined project management up to on-time delivery

Dedicated Design Center

- Dedicated team per customer roadmap • Flexibility & scalability
- Delivery responsibility with Eteros • Virtual team or physical office

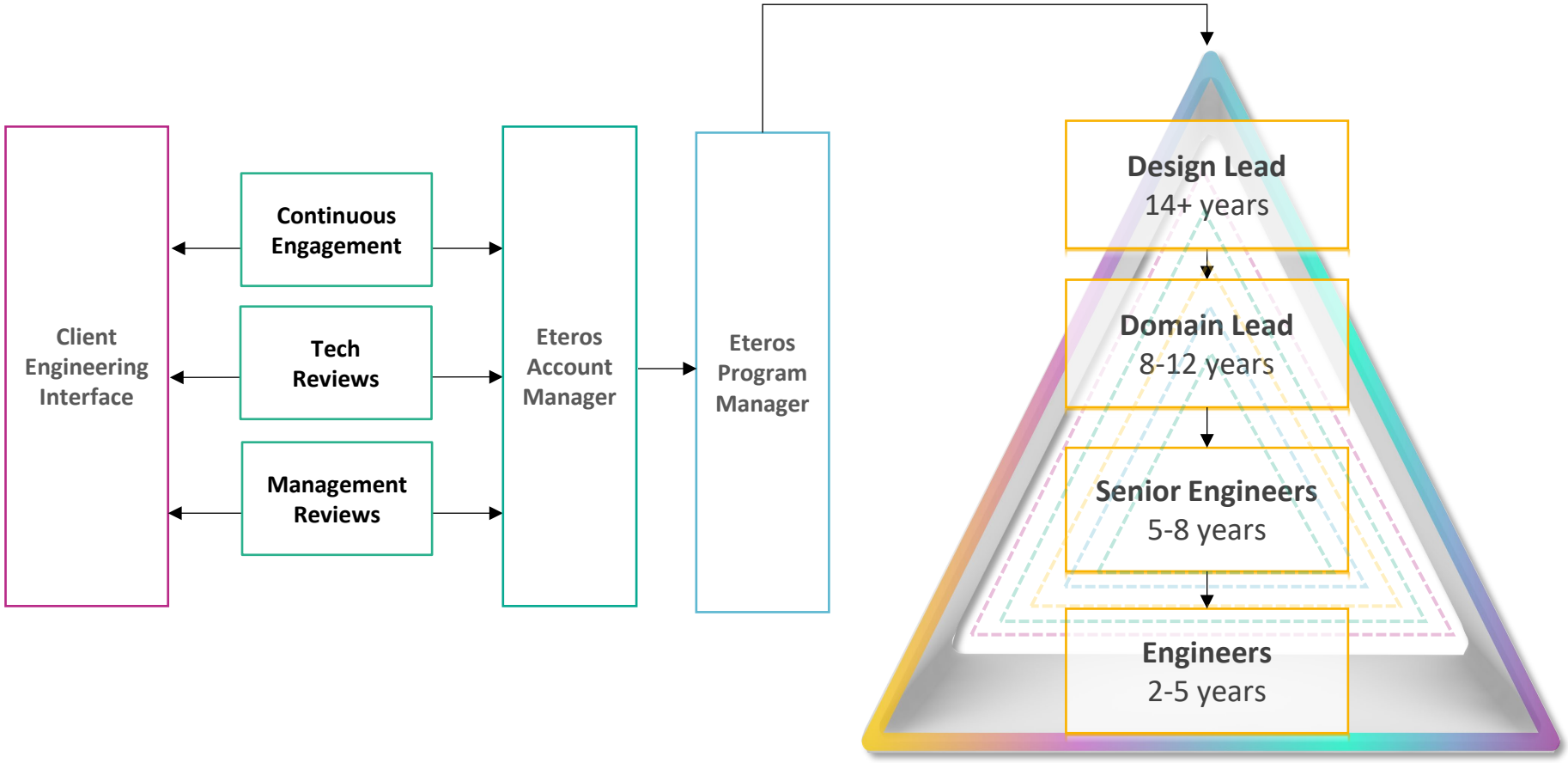
Staff Augmentation

- Support customer’s existing engineering teams
- Eteros engineers interact directly with counterparts

Build Operate Transfer

- High-caliber team for specific customer needs
- Execute project for fixed duration • Transfer team to customer

Engagement Model for On-Time, On-Cost Delivery



Eteros Team: Right Expertise + Right Sized Team

Our Leadership

Experienced Leadership

Jai Durgam, Co-Founder
30+ years, GlobalFoundries, Synopsys,
Scintera Networks, National Semi

Vishal Abrol, Co-Founder
25+ years, Cadence,
Mentor Graphics, Hughes

Sudheer Reddy, Co-Founder
20+ years, Intel, Aricent,
ST Microelectronics, Qualcomm

Manjunath V, Physical Design
25+ years , Signoff Semi
Open-Silicon, Cadence, Intel

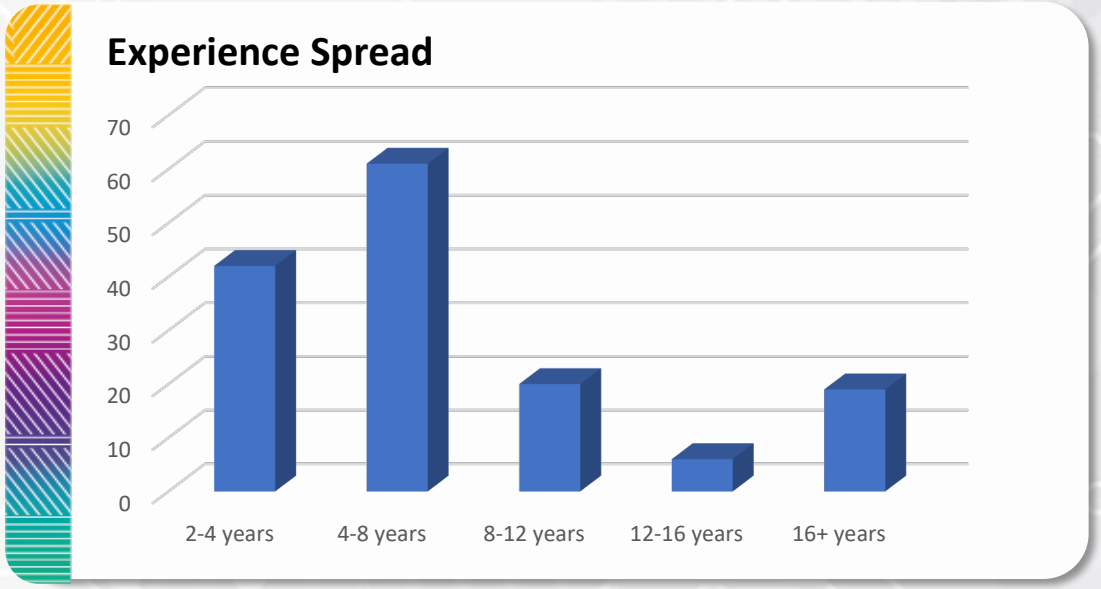
Dharanendra K, Verification
22+ years, Cypress, Cisco, IBM

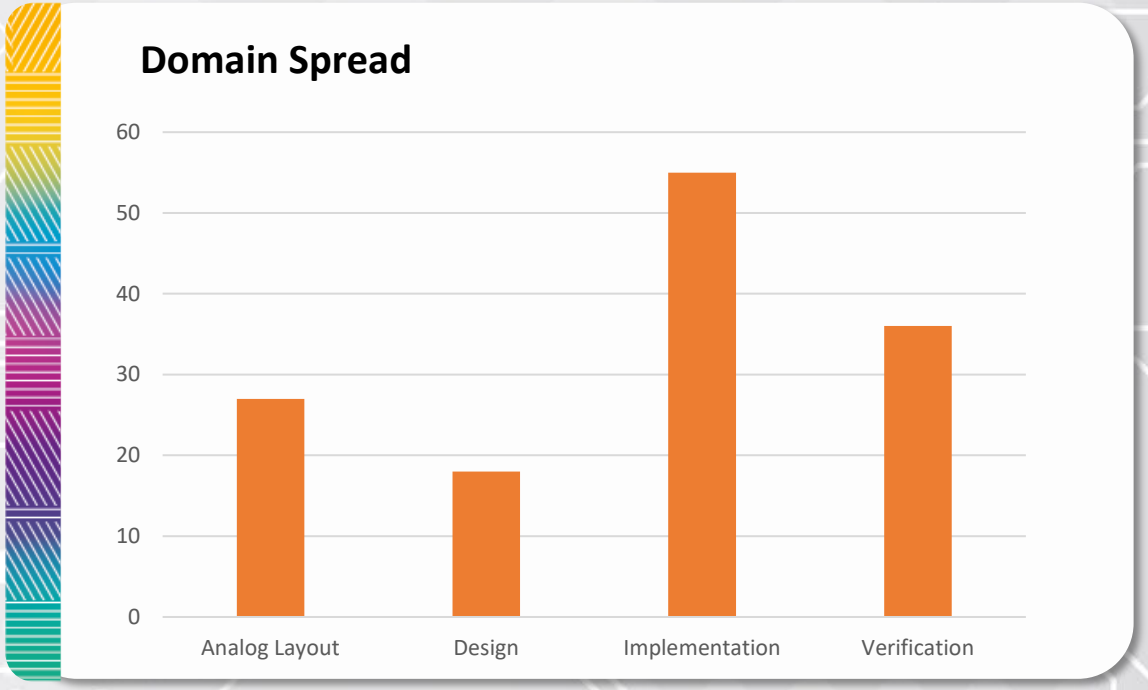
Mohd. Maaz, Layout
16+ years, Mirafra, Cyient,
National Semi

Ankit Khare, DFT
18+ years, NXP, Qualcomm,
ST Microelectronics

Suresh N, Analog Design
18+ years, SNPS, Intersil,
Qualcore

Engineering Depth & Spread

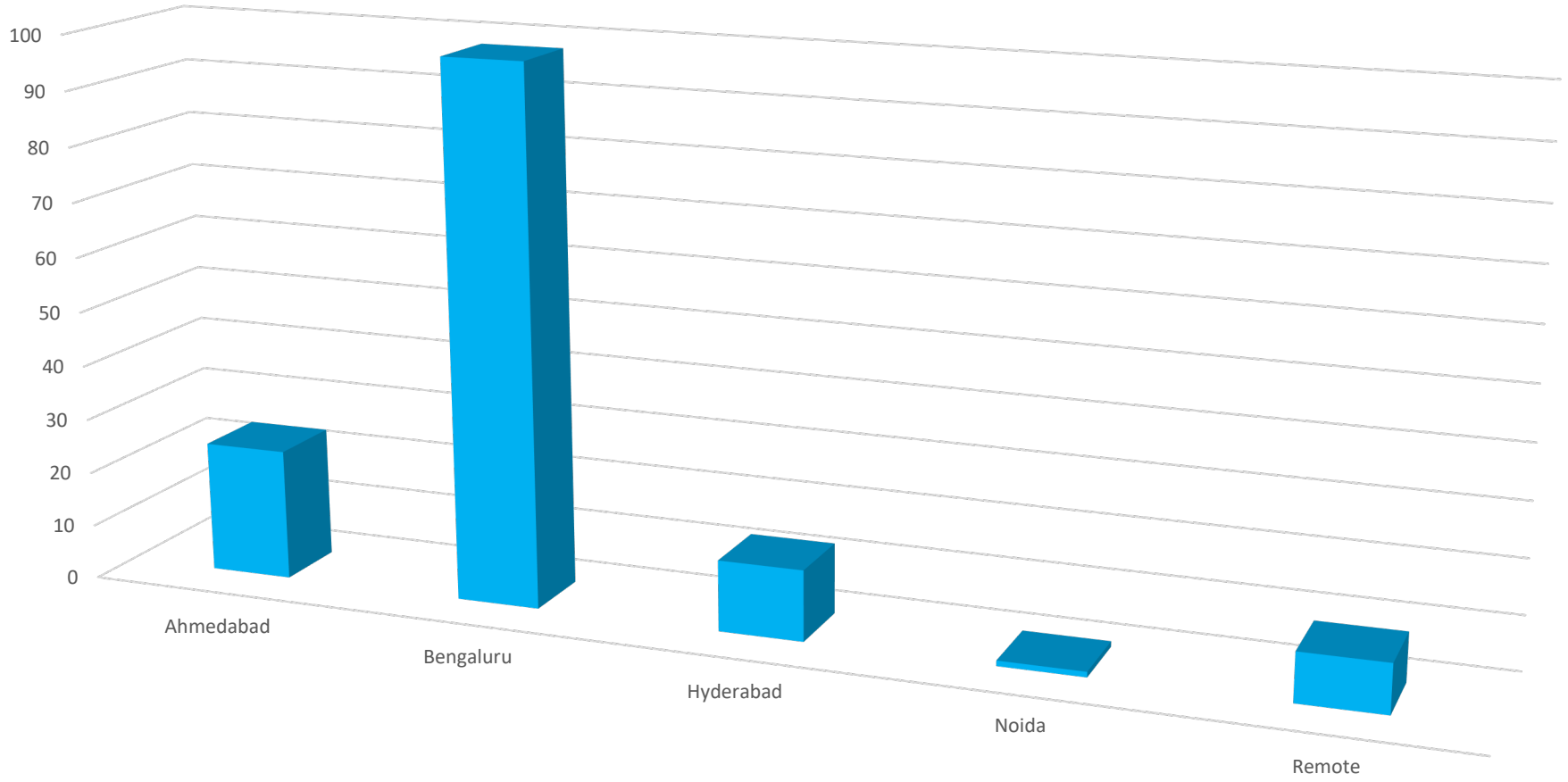


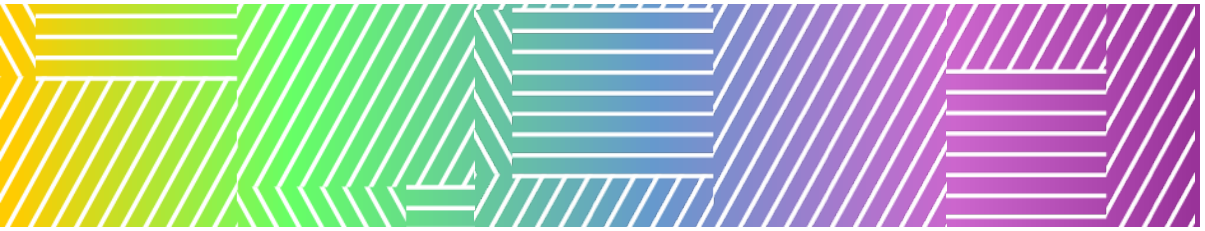


~6.5 Years

Average engineering experience

India Engineering Locations

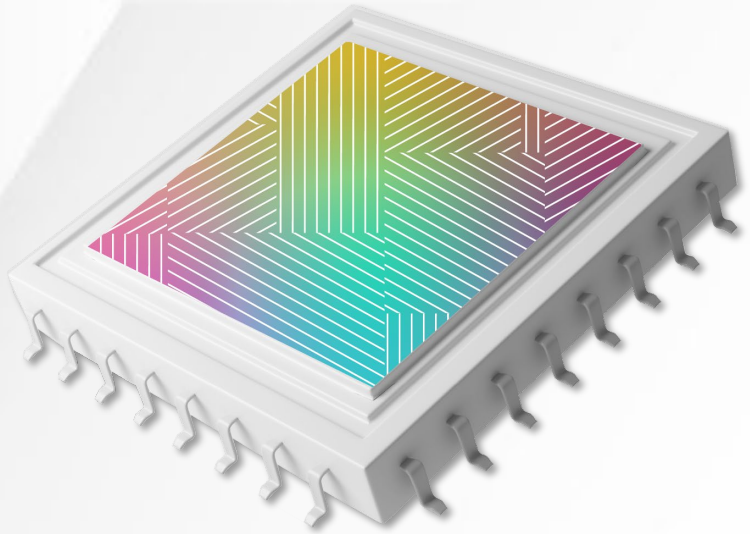




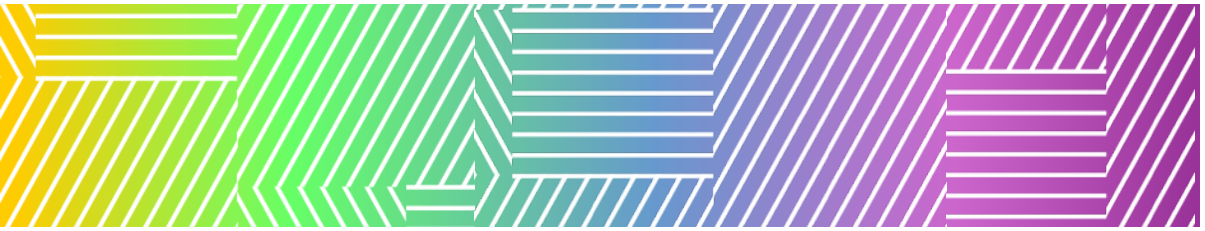
Eteros Advantage

The Eteros Advantage

- End-to-end silicon design
- Experience delivering for top-notch start-ups and large companies
- Proven expertise in Automotive, AI, Datacenter SoCs
- Worldwide talent pool to attract and deploy the best talent on-demand
- Differentiated business model: Right expertise + right-sized teams for on-time on-cost delivery



On Time. First Time Right. Every Time.



From Sub-Systems to SoCs

Areas of Focus: Physical Design and DFT

Physical Design & Sign-off

- Synthesis, Logic Equivalence Checking
- Timing constraints development and validation
- Full-chip Floorplan – Partitioning, IO Layout, Bump/RDL
- Block-level implementation –
- PPA Optimizations, MMMC optimizations
- Block-level and Full-chip Sign-off
  - STA and timing closure
  - IR-Drop, EM, ESD analysis and closure
  - Physical Verification – DRC/LVS/ERC/DFM
  - Define sign-off methodologies
- Full-chip integration and Sign-off
- Methodology development, automation

Design for Test (DFT)

- Defining complete DFT architecture
- Boundary Scan, JTAG, iJTAG implementation
- Scan insertion
  - Hierarchical/Flat strategies
  - Compression, OCC implementation
- ATPG
  - Pattern generation and Simulations (timing/no-timing)
  - Test point insertion, coverage improvement
- Memory BIST generation, integration and simulation
- LBIST generation and integration and simulation
- Test-mode timing constraints generation and timing closure
- Verification at all phases to ensure final sign-off
- Post-SI
  - Tester debug, silicon bring-up
  - Failure analysis assistance and yield improvement

Areas of Focus: Analog

Design

- Technology nodes: 5nm, 7nm, 12nm, 14nm, 16nm and above
- High speed analog layout
  - 56G & 112G Serdes, High-speed TX/RX
  - ADC, DAC, PLLs, LDO, VREG, BGR, PI, PIMX, Oscillators, Sensors etc.
  - DDRs – DDR54, LPDDR4X
- AMS Modelling and AMS Verification

Layout

- AMS, RF Layout, Digital, Custom Digital layout
  - Technologies – 5nm to 180nm and above
  - Foundries – TSMC, GF, SMIC, Samsung
  - IPs – High-speed, RF, High-density, Memories, Standard cells
- AMS CAD
  - Automation and flow development

Areas of Focus: Design Verification

Design Verification

- SOC Level verification
  - Test Plan to Post-Si end-to-end verification
    - Environment creation and automation
    - Testbench/Testcase development
    - Pre-SI verification - Coverage analysis, Regressions
    - Gate-level-Simulations
    - System level validation
    - CPU based verification, cache-coherency
    - Assertions, Assertion based verification
  - C/C++/SV/OVM/UVM based verification
- IP Level verification
  - Feature testing and verification
  - IP to VIP development and integration
  - SOC integration verification
- AMS Verification
  - Digital-on-top and analog-on-top mixed mode
  - AMS modeling and verification
- Flow development, documentation and training

- High-speed protocols
  - USBx, PCIe, SATA, SPI, MIPI, CSI, RapidIO
- Memory interface/SSDs
  - NAND, DDRx, SD, eMMC and flash controllers
- AMBA protocols
  - APB, AHB, AXI and AHB-lite
- Domains
  - 5G NoCs, Modems, Networking, Ethernet
  - Image Processing, Edge computing
  - CPU – ARM, Faraday processor

Contact us

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LinkedIn

Thank you
धन्यवाद
شكراً
Merci
תודה
谢谢
Toda
Bedankt

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