Emulation in your verification & validation strategies

How best to deploy emulation to sign off on HW & SW

- HW verification, HW/SW validation, Prototyping

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Verification Trends: Process

Standardization of the SoC Verification Process

- IP Challenges
  - Effective test bench and test creation
  - Covering corner case effectively
  - Getting to Coverage Closure faster
- Subsystem Challenges
  - Verify all interactions and functionality
  - Generate various key tests to verify performance
  - Cover all states and transtions for cache coherent interconnect
  - Create end-to-end scenarios and debug interactions of network
- SoC Challenges
  - Connect 1,000's of blocks without error
  - Verify clock domain crossing problems
  - Verify low power circuitry and intent
  - Verify no X's due to RTL semantics
  - Bare Metal verification of my CPU
- System Challenges
  - Executing and Debugging drivers and real application software
  - Executing large amounts of real data through subsystem or large block
  - Execute and measure system performance with the software executing?

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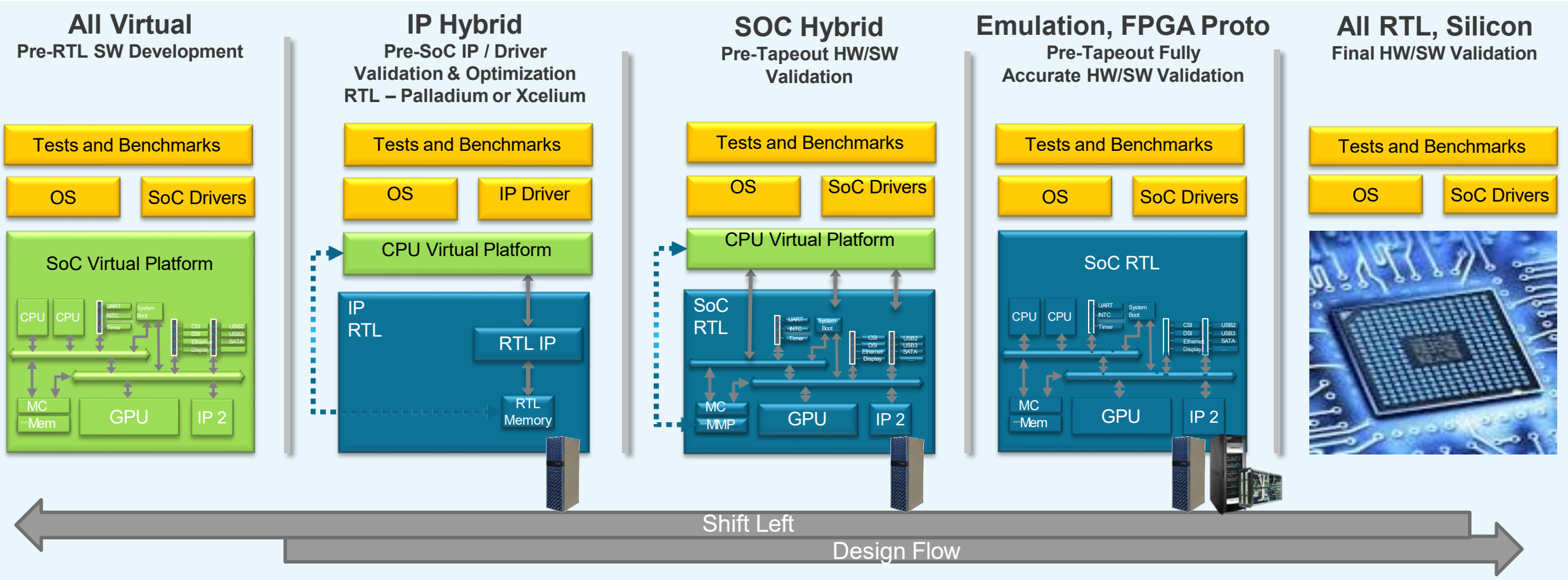
HW/SW verification & validation

Using virtual platforms and hybrids to accelerate SW development and HW/SW validation

Color Code: SW stack; Virtual Models - VSP; RTL Models -



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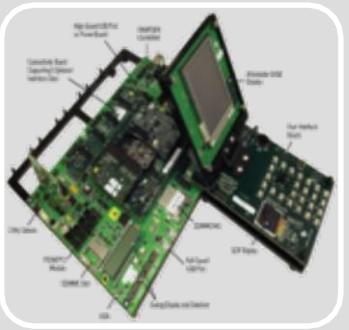
A Continuum of Dynamic Engines (e.g. Cadence)

Verification and software platforms need to interoperate



Virtual Platform

Almost @ speed
Pre-RTL
Less accurate
TLM HW Debug
Great SW debug
Easy replication

Less HW detail
Slower with detail

HDL Simulation

KHz Range
Early RTL
Golden Reference
Best HW debug
Limited SW Debug
Easy replication

Mixed-abstractions
Slow SW execution

Acceleration Emulation

MHz Range
Early RTL
Min RTL mods
Detailed HW debug
Great SW Debug
Harder to replicate

Datacenter access
Contested Resource

FPGA Prototype

10's of MHz
Later RTL
Some RTL mods
Some HW debug
Great SW Debug
OK to replicate

Harder Bring-up

Prototyping Board

Real time speed
Fully accurate
Actual Silicon
Difficult HW debug
OK SW Debug
Easy to replicate

HW changes hard

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Trade off performance & debug etc

Performance

Server

Xcelium™
Simulation

Custom Processor

Palladium® Z1
Emulation

FPGA

Protium™ S1
Prototyping

Debug Flexibility & Compile Time

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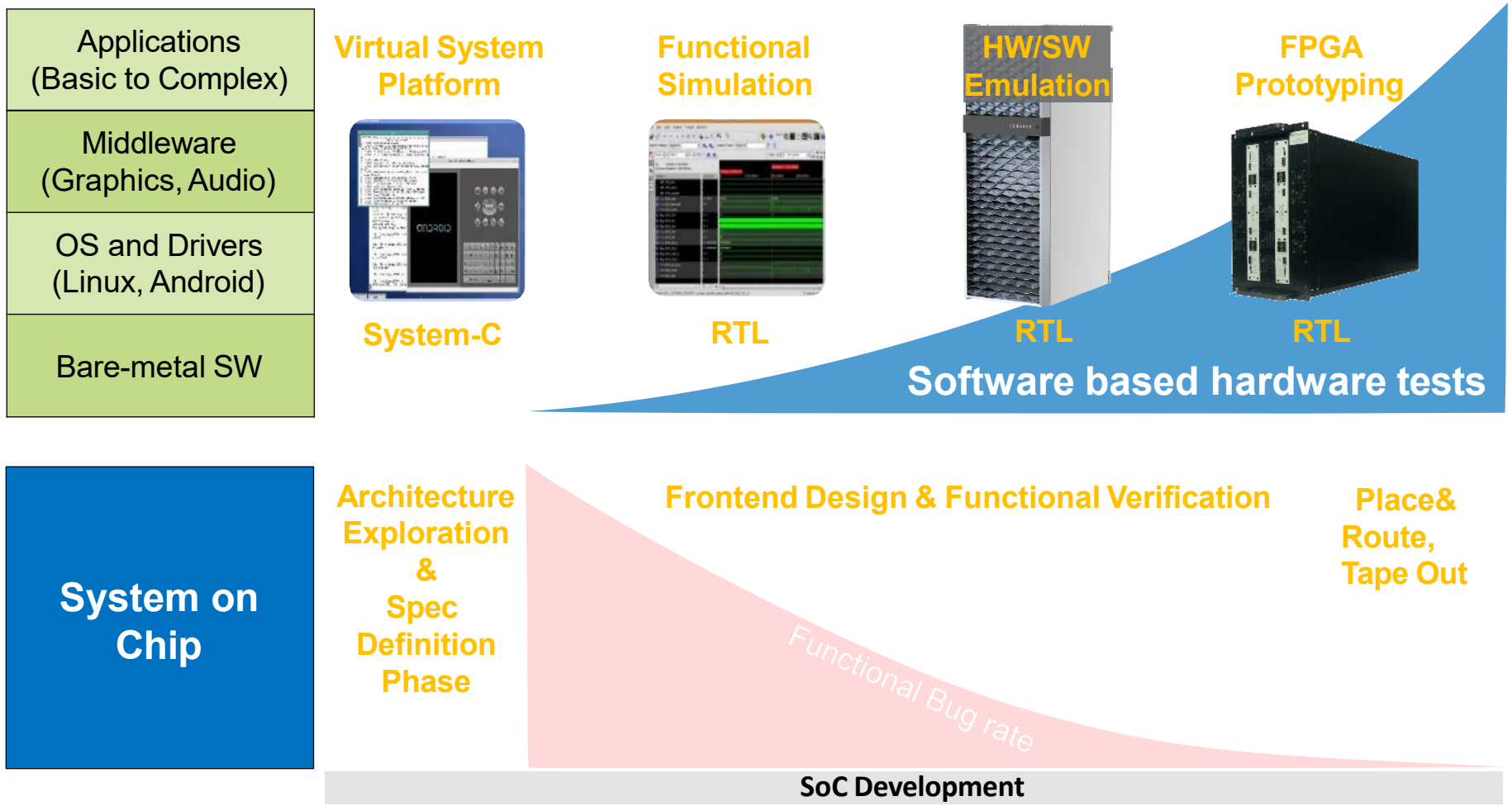
Hardware/Software Co-Verification during SoC Design



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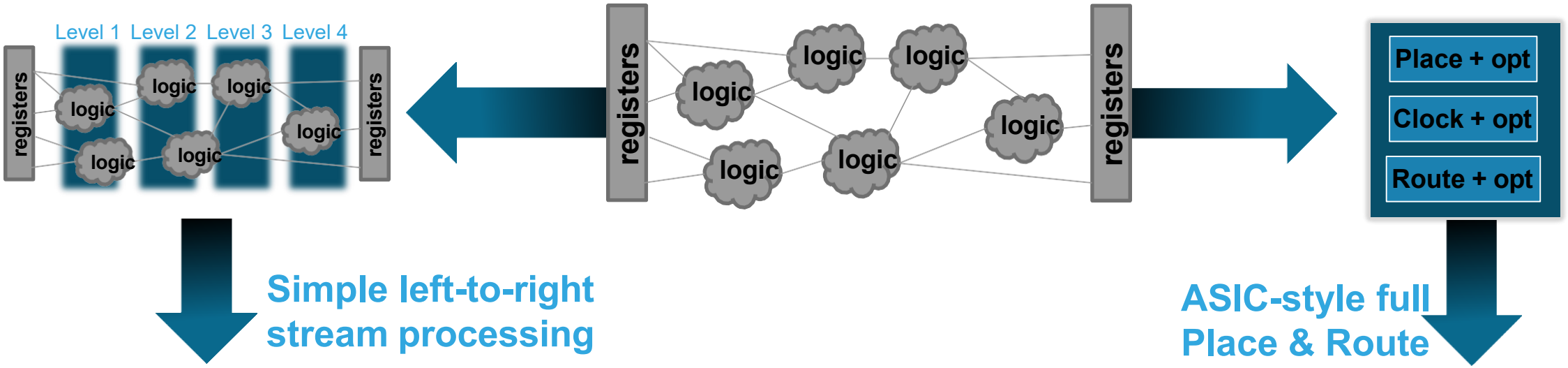
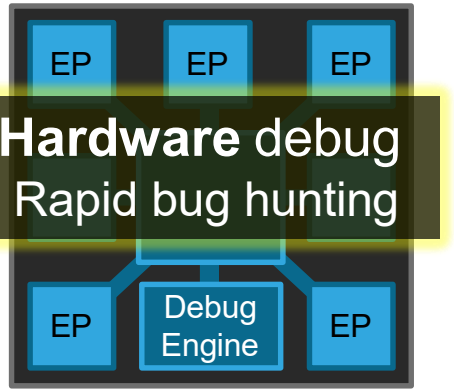
Combining Emulation and Prototyping



Simple left-to-right stream processing

ASIC-style full Place & Route

Emulation Processor



Hardware debug
Rapid bug hunting

1MHz

- Fast compile
- Predictable compile ("If it compiles it runs")
- "Full Vision" debug

5-20MHz

- Slow compile
- Compile may need tuning to close timing/routing violations
- Limited debug

Xilinx FPGA

Software bring-up
Deep bug hunting

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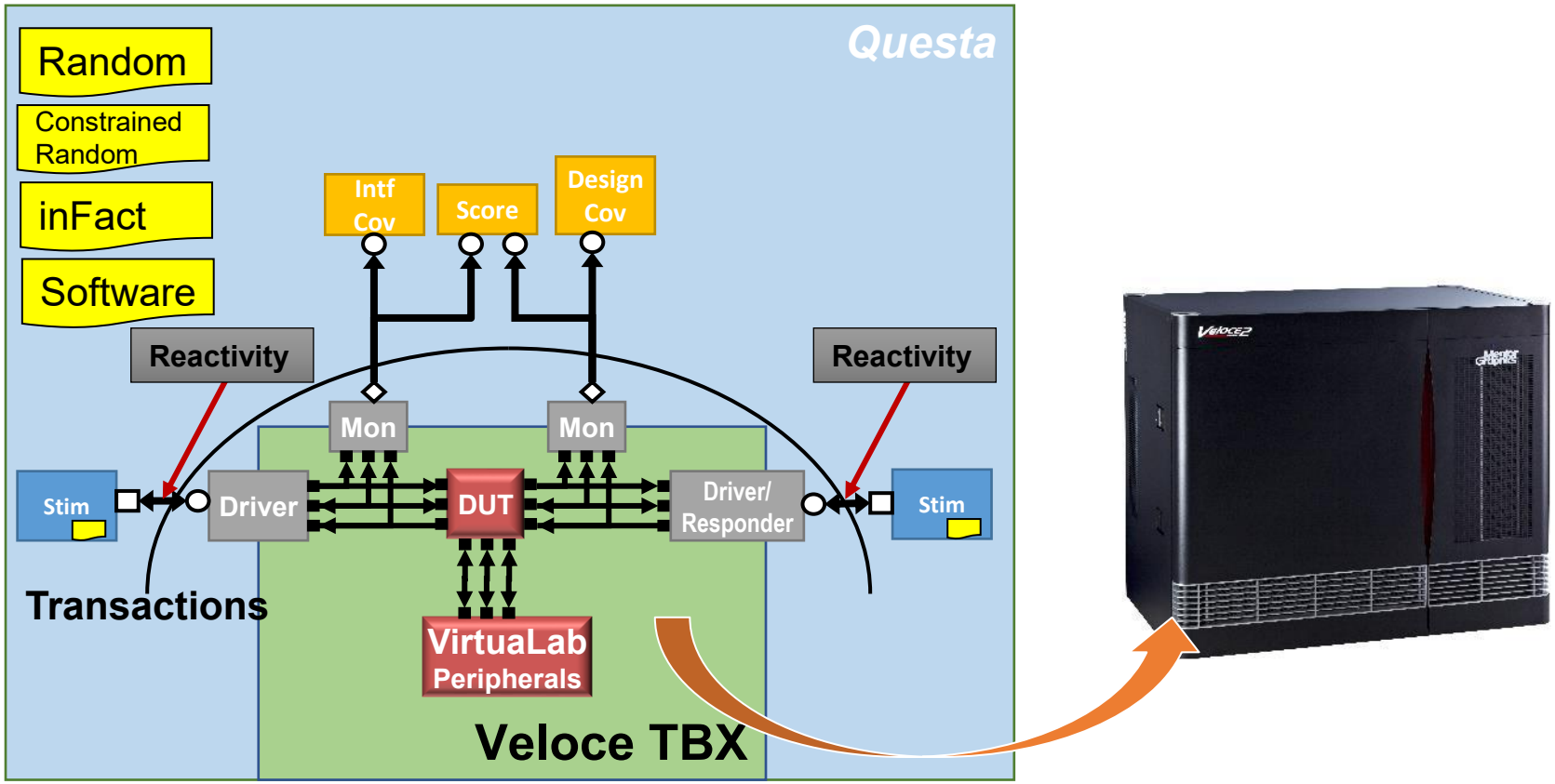
Questa + Veloce = Veloce TBX

High Performance for SoC and System



- One testbench for simulation and acceleration

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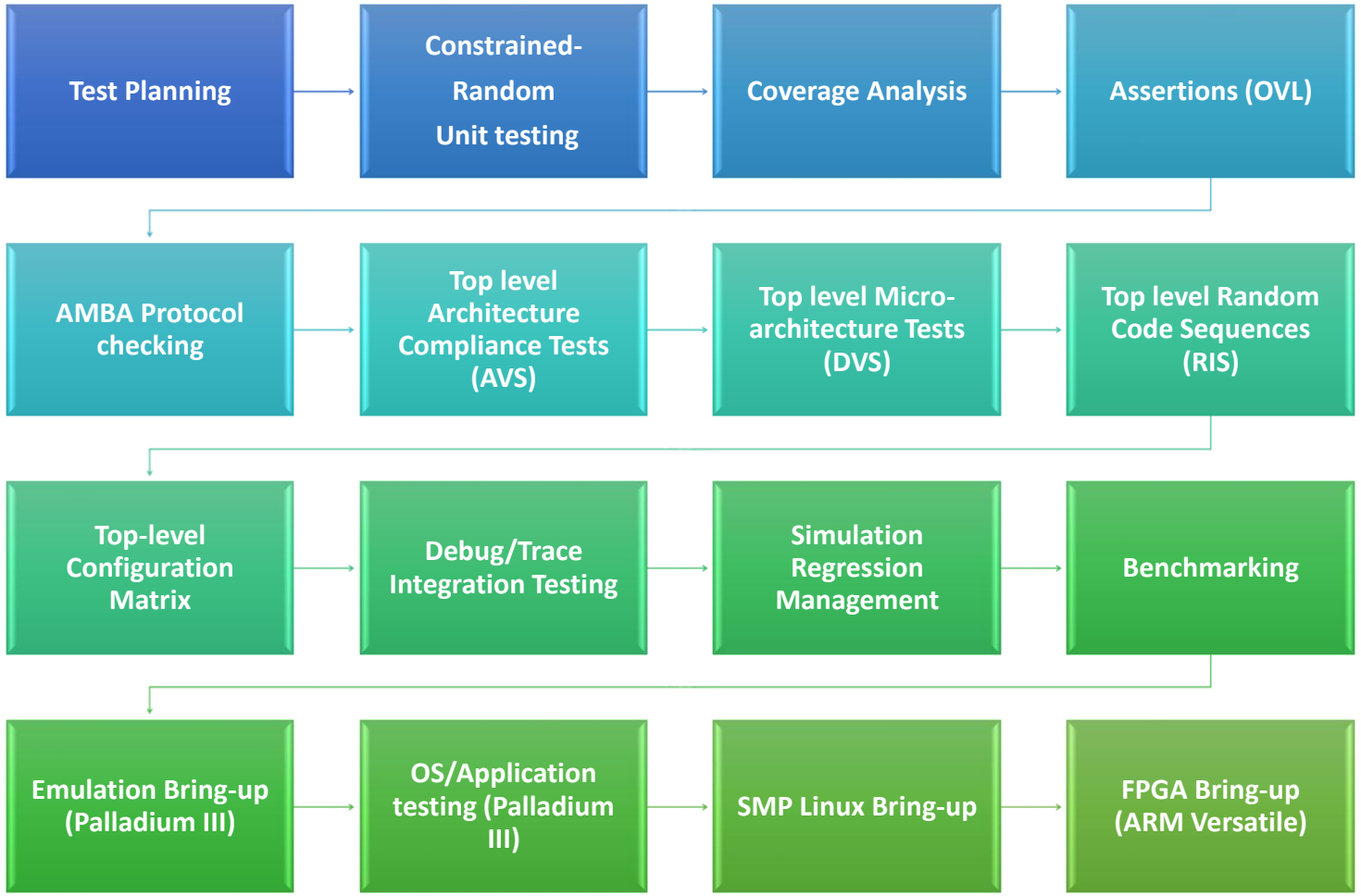
Cortex-A9 MPCore Verification Flows



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System Validation

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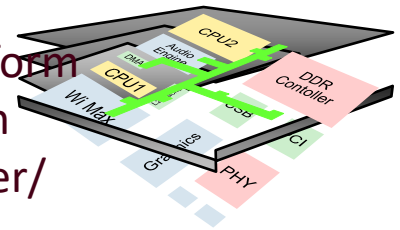
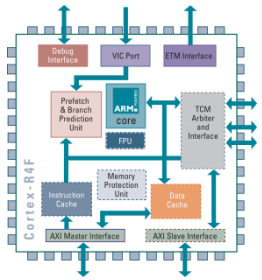
System Validation: the Verification Queue

Integrated Product (Partner/ OEM)

SoC Platform (Platform Developer/ Partner)



IP Block (IP Provider)



Production Silicon/ Product Release (System QA Testing)

Prototype Silicon (software development and Full system testing)

System and Device Testing

SOC Validation (FPGA, Emulation)

SOC Integration Testing (Simulation)

Target SoC/ Integration DV

System Level Bring Up (FPGA, Emulation)

Top Level AVS/DVS/RIS

CR Unit TB

Assertions Coverage Formal

Pre-Silicon IP Block DV

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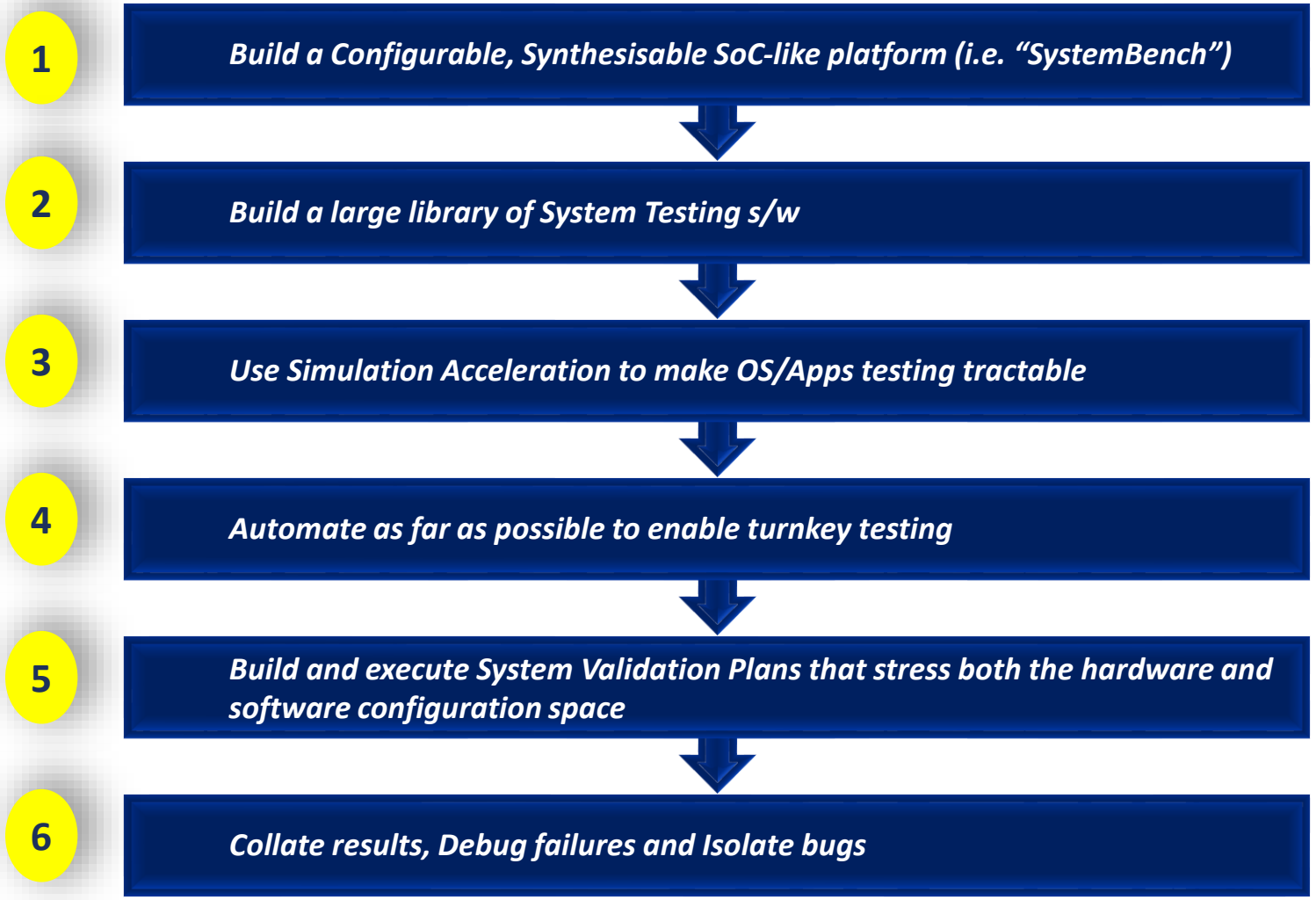
System Verification Approach (Steps):



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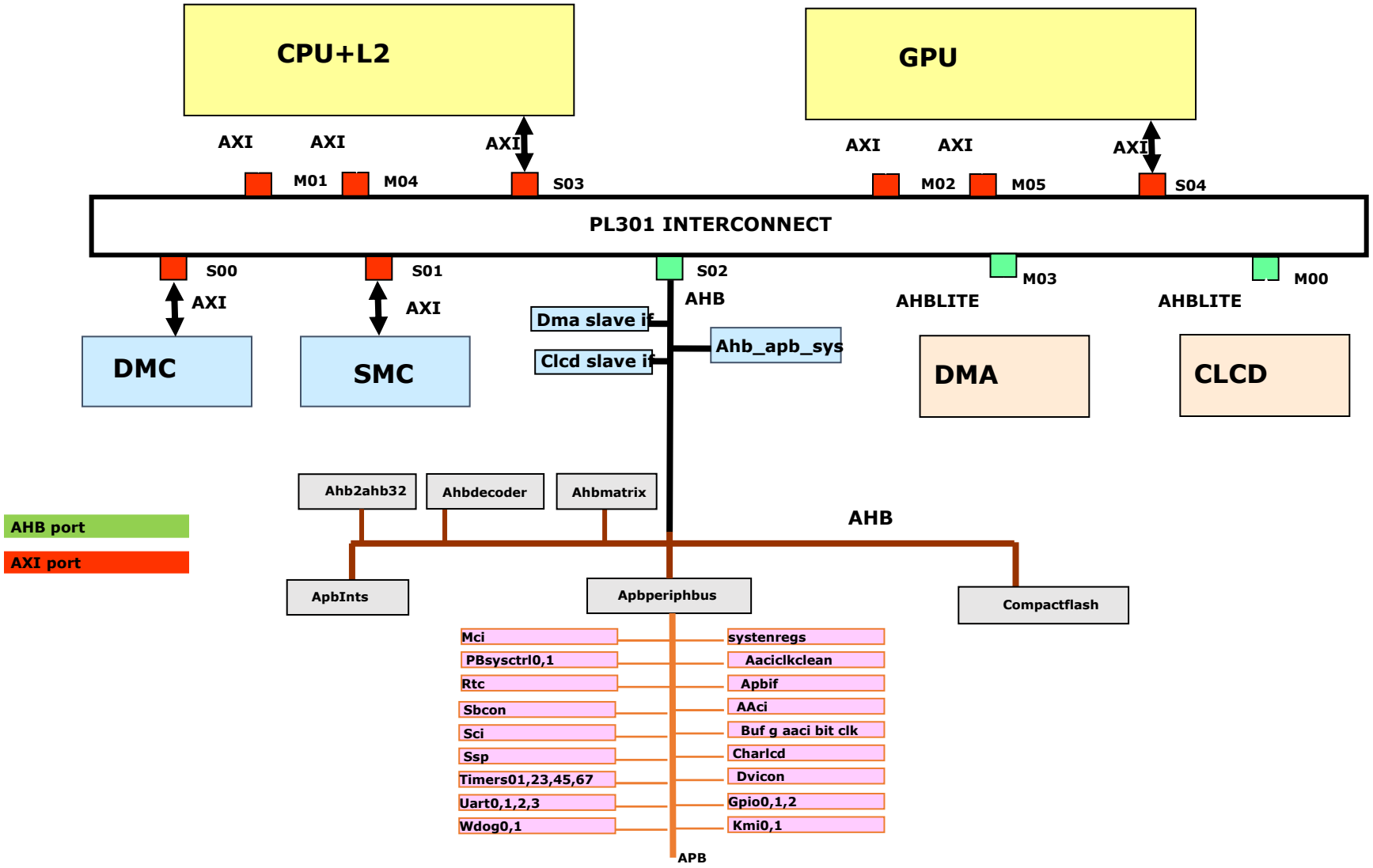
Arm SoC verification



Note :This is not a comprehensive figure which shows all the blocks rather it highlights the bus ,interconnect view of systembench

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Emulation and Validation Services for Mobile SoC

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Client:	**SoC Mobile Manufacturer**
Industry:	**Semiconductors**
Business Model:	**Offshore**

Background

- The customer selected Tessolve to perform validation using FPGA-based emulation of their mobile phone SoC

Technical Solution

- Understand the customer flow of emulation
- Write a wrapper for the RTL for FPGA porting
- Generate FPGA memory compatible with the RTL
- Write time and clock constraints for synthesizing design
- Synthesize the design using Simplify premier and analyse the timing of the design
- Partition the RTL into multiple FPGAs
- Generate the bit files for all the FPGAs
- Iterate
- Validate the SoC design by running software applications on the FPGA

Results

- Tessolve were able to discover multiple bugs in the RTL and allowed the customer to validate the SoC design through execution of software. The FPGA platform could then be used for further software development.

Benefits to Customers

- The FPGA emulation helped the customer to meet challenging product release schedules
- Complex hardware system functionalities were verified in advance of tape-out to secure first time working silicon
- The FPGA-based software validation reduced the overall product development cycle
- Tessolve completed the project without exceeding the original budget and timescales.

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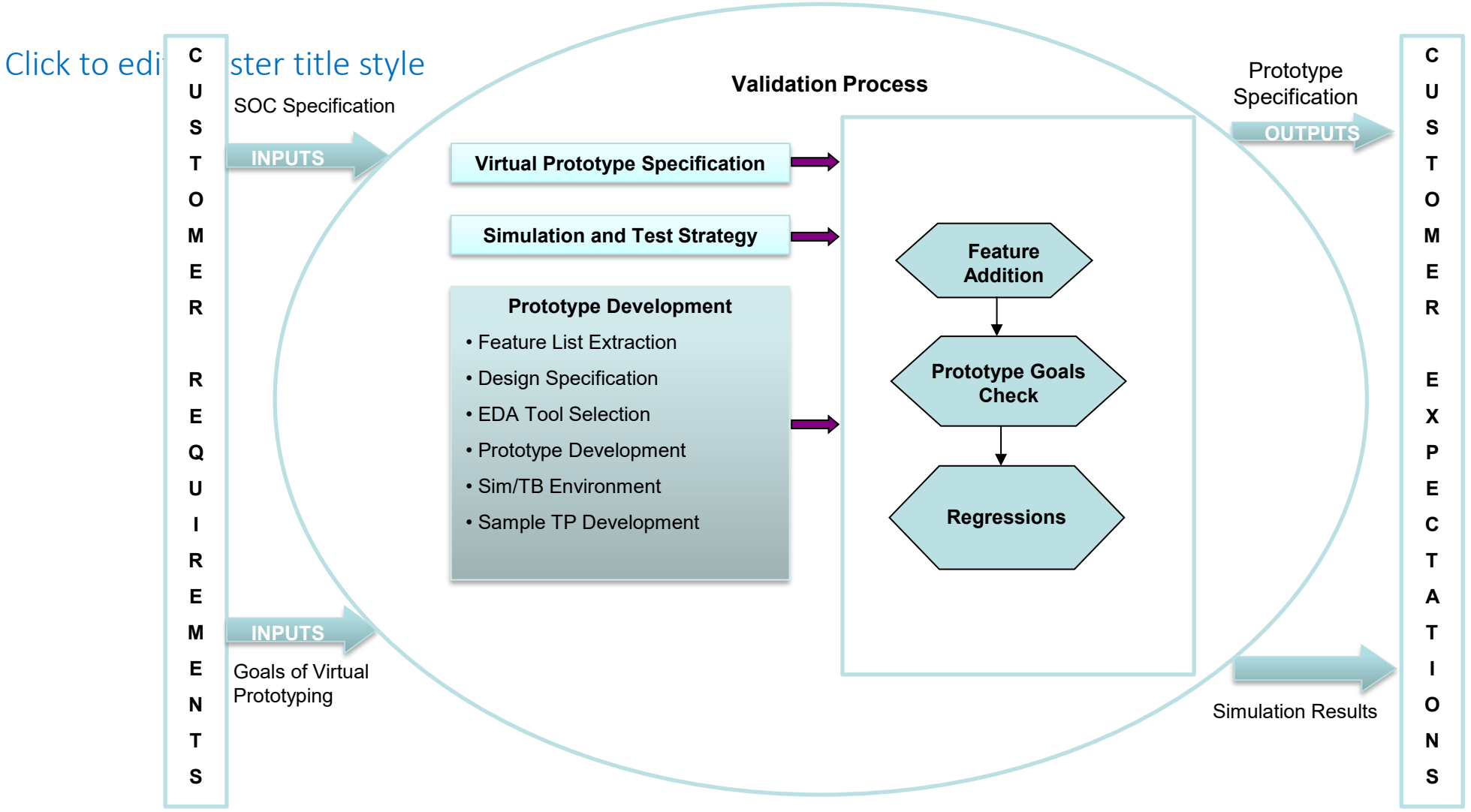
FPGA - Virtual Prototyping Process



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Virtual Prototype Development

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Client:	Electronics Major
Industry:	Wireless
Business Model:	Offshore

Goals of Model Development

- **Virtual Prototype For Early SW Development**
  - Diagnostic SW Development
  - uBoot with Peripheral Driver SW Testing
  - ARM DSM and TI 64X+ Model provided by Vendor
  - All Peripheral Controller with Register Modeling Done
  - Communication between Interconnect via TLM
  - SW tested on prototype used for Board Level Silicon Testing

- **Virtual Prototype For Architectural Exploration**
  - Operational Delays in Peripherals Modeled Same as Specification
  - Response Times were modeled exactly as per specification
  - Complex Models like IPSEC, EMAC converted to SystemC Models using Carbon Tools
  - Interconnect Was a pure TLM Model. Delays of Interconnect added to the peripheral models
  - Write a wrapper for the RTL for FPGA porting.

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Virtual Prototype Development (Continued..)

Click to edit

Client:	Electronics Major
Industry:	Wireless
Business Model:	Offshore

- **Engagement**
  - Feature list extraction for Prototype Development
  - SystemC Model development for peripheral controllers
  - SoC Designer Virtual Platform development for building Test Programs and architectural Exploration
  - Test Programs in C for testing the Peripheral controllers
  - Test Program Debugging
  - Running tests on actual board
- **Key Success Factor**
  - Commitment
  - Competent Project Management
  - Planned Ramp Up & Down
  - Knowledge retention and management
  - Operational Efficiency
- **Technology**
  - ARM DSM, SystemC Models of all Peripherals
  - RTL -> SystemC Converted models (using carbon)
  - Virtual platform built using ARM's RealView SOC Designer
  - Simulation using ARM'S RTOE
  - Debugging – Waveforms, RVDS
    - ARM's Realview SOC Designer
    - RVDS, RTM
    - RTOE
    - Carbon
- **Benefits to Customer**
  - Early development of test programs on virtual platform which can be used in Actual Hardware
  - Architectural Exploration
  - Verification of Complex RTL IP Blocks

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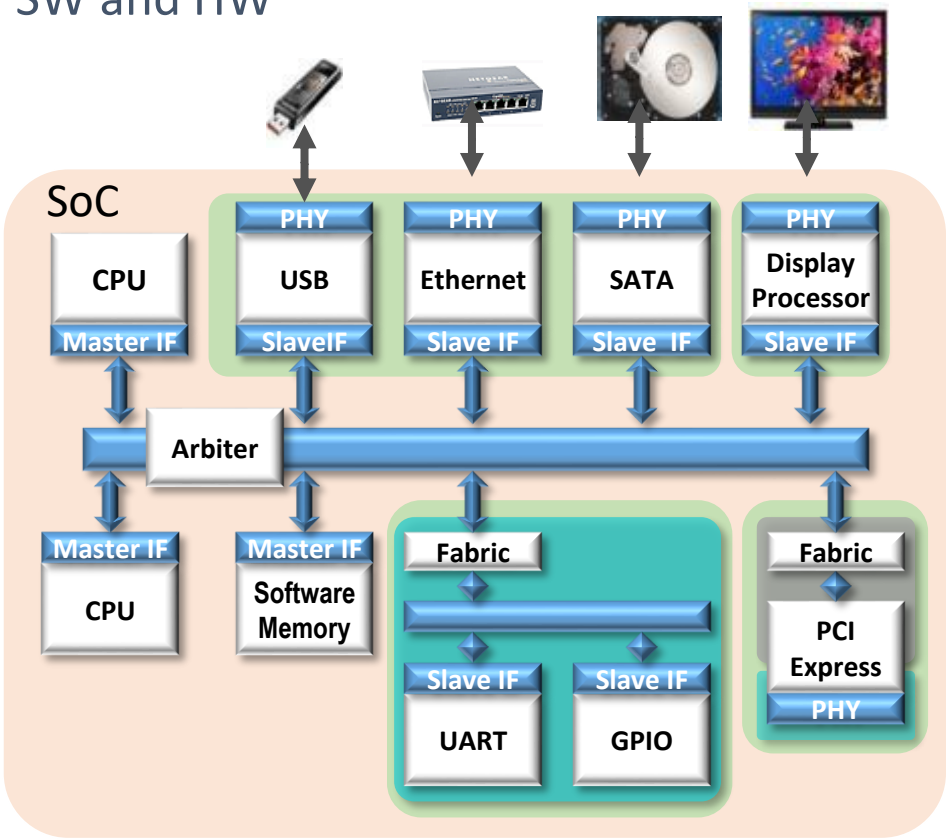
Verification Impact: Emulation

Emulation is becoming mandatory for System Level Verification

- SoC capacity and performance requirements exploding
- SoC verification requires real SW with HW
- Power management implemented in SW and HW
  - Critical to verify together
- Verification must flow smoothly from Subsystem to SoC



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Summary

- We have seen how best to deploy emulation to support first-time working solutions for HW+SW
  - HW verification
  - HW+SW validation
  - Prototyping

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