Alpinum VLSI Expertise

Mike Bartley, CEO

Verification Services

- RTL Design and Verification
- Physical Design
- Analog Circuit Design and Layout
- SIGN-OFF Expertise
- Test Solutions and Services(DFT)
- Embedded System & Controls

RTL, DfT and Embedded Services

Synthesis
- DC/RTL Compiler
- Physical Aware Synthesis
- Low Power Aware
- DFT insertion
- Logical Equivalence

Pre/Post STA
- Timing budgeting at SOC
- Constraints Development
- IO timing closure
- Timing ECO generation
- SOC / Subsystem Timing closure

DFT
- Scan Insertion
- ATPG
- Test pattern generation and simulation
- Coverage improvement
- IDDQ, BIST, BSCAN
- DFT Spyglass checks
- Test mode timing constraints

Placement & Route
- Floor planning and Partitioning
- Clock-Tree Synthesis
- Multi-Mode Multi-Corner Opt
- Power Optimization
- High Utilization
- UPF/CPF aware flows

Sign-Off
- Hierarchical Designs
- Flat STA closure
- Physical Verification
- IR and EM checks
- SOC Low Power checks
- SI and PI

Embedded Development
- Software Development
- Testing, Validation and Verification
- MATLAB and Simulink
- Application Development
- Firmware, FreeRTOS
- C, C++, QT Framework with QML, MQTT
- Linux , BSP, Yocto Application Development
- Safety and Security

Physical Design Services

ASIC Design

- Custom Chip
- Mixed Signal Integration
- Low Power Design
- High Frequency Analog Design

Analog & Mixed Signal Layout

- SOC Integration
- PLL
- DAC
- ADC
- CLOCK SYNTHESISER's

Custom Layout

- Analog routing
- Memory layout
- Standard cell
- Custom Digital

PDN

- IR Drop Analysis.
- EM analysis.
- Rush Current Analysis.
- Generating EM-IR models.
- Defining EM-IR flows & Sign-Off methodologies

FEV & VCLP

- Static Low power checks at SOC / Subsystem / Block level.
- Power Intent Verification at Designs
- Logical Equivalence checks - RTL to RTL , RTL to Netlist &
- Netlist to Netlist
- Low power enabled Equivalence checks

DRC & LVS

- SOC level DRC and LVS checks
- PERC checks
- Electrical Checks
- ESD checks

Case Studies

AMD

Project: Navi31, Navi32, Navi33, Navi36, Navi3C, Navi44, Navi48, Navi4C, Navi4X, MI200, MI300, MI350

Work Done by us:

- RTL Design
- Functional Verification
- Formal Verification
- Emulation
- Design For Testability
- Physical Design
- Analog Circuit Design
- Analog Layout

Project Duration: 48 months

INTEL

Project: Laguna, Malibu

Work Done by us

- RTL Design
- Verification
- Design For Testability
- Physical Design
- Analog Circuit Design
- Analog Layout

Project Duration: 28 months

Google[GChips]

Project: ACR CPP, FM4, FM7, FP8, SM7

Work Done by us

- RTL Design
- Functional Verification
- Formal Verification
- Design For Testability
- Physical Design
- Analog Circuit Design
- Analog Layout

Project Duration: 42 months

IPs

Interface IPs

- PCIe Gen 7/6/5/4/3/2/1, CXL 2.0/3.x, UCIe 2.x/1.x
- HBM, LPDDRs & DDR5/6, UFS, NAND Flash controllers
- USB 4.0 Controller, 800G Ethernet Controller,
- MIPI CSI, DSI and I3C IP Controllers
- UART, SPI/ QSPI, I2C, CAN

Bluetooth Low Energy & Other IPs

- BLE Signal chain Tx & Rx in 22nm process
  - Tx chain <2.5mA @0 dBm o/p power @ 0.75V supply. O/P power range support -8 to 8 dBm. Scalable to 20 dBm.
  - Second TX chain with 16dBm o/p power with 45% and higher power efficiency
  - For Rx chain we are targeting ~1.8 mA or less current from 0.75 V supply. Sensitivity better than -96dB at chip port.
  - Modem current can be range of 0.6-0.7mA from 0.75V.
  - We will extend this design to BLE Audio
  - Architecture supports extremely low, best in class connected idle current numbers
  - We can support on-chip Intelligent power management (IMPU) design to support the full SoC
  - Architecture is complete. Design in development phase

IPs

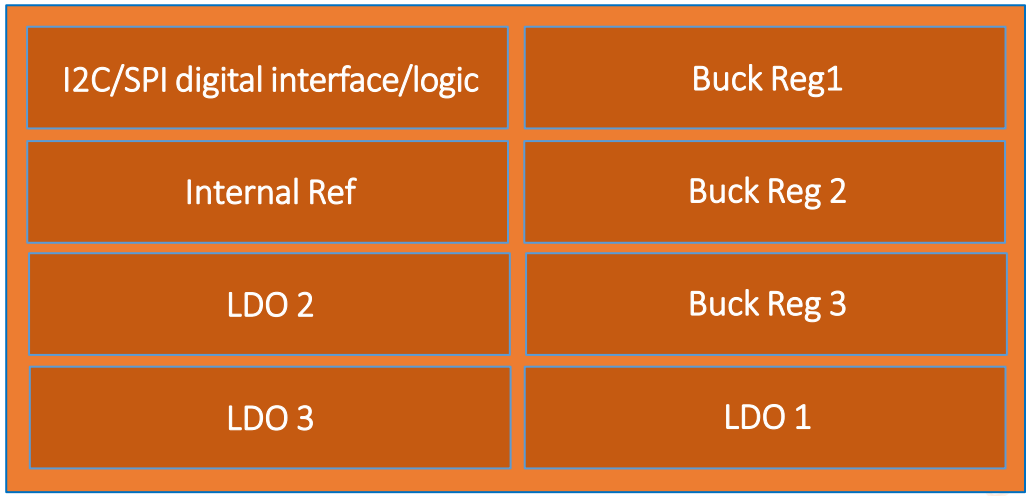
Wireless IPs

- ADC
  - 12/14 bit, 1 Gbps ADC
  - 12/13-bit 320/640 MHz SAR for WiFi6E and WiFi7 applications
  - 12/10-bit 80/160MHz low power SAR
  - 8/7/6 bit, 1 Gbps SAR
- DAC
  - 12/14bit 1Gbps
  - 6/7/8 bit, 1 Gbps
  - 12/10-bit 200/400MHz
- LC and Ring PLLs
  - *2.4-3.2 GHz* LC PLL design with best in class ultra low phase noise
  - *4-7.5 GHz* and 8–12.6 GHz LC PLL design
  - Ring and Digital PLLs for SoC and other clocking applications
  - Low area, low power, wider tuning range designs
  - Supports Spread Spectrum & Dithering
- BLE Tx and Rx chains
  - Tx chain <2.4mA @0 dBm o/p power
  - Rx chain <1.5mW with -96 dB sensitivity @ 1mbps
- WiFi 6E and WiFi 7 signal chains
- Wakeup Receiver / Wireless (Wi-Fi) sensing

General Purpose IPs

- Reference Circuits
  - Bandgap, voltage and current reference circuits
  - General purpose Monitor ADC with
    - 12-bit SAR, low power
    - Sampling rate 1-10 Mbps
  - 14/12 bit DACs
  - Crystal oscillator
    - Fast start-up and wide xtal frequency range support
    - Low Phase noise additions
  - clocking circuits and Oscillators
    - General purpose PLLs and DLLs
    - RC oscillator(s) with frequency tuning and self calibration
  - Detectors
    - Supply Glitch Detector
    - ADC based Temperature Sensor
    - PVT Detector
  - Specialized IO designs – based on customer request
- Specialized Analog Mixed signal IPs
  - SERDES Design- -> Our design has good knowhow and capability of 10Gbps to 56Gbps design

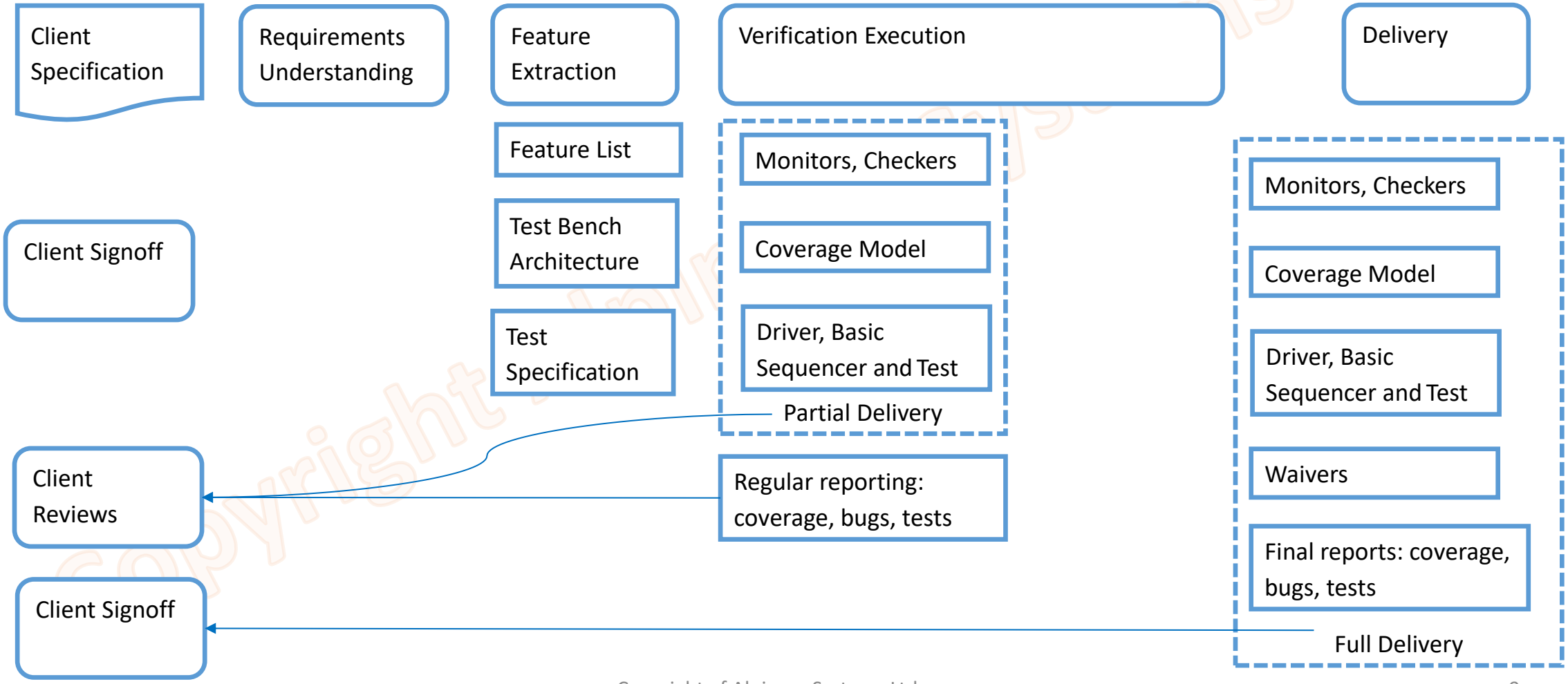
Customizable-Power Management IC



- Single supply design with multiple outputs
- Customer specific customization available
- Buck_REG1
  - Input supply 3V-> 5V
  - Output voltage range -> 0.75V-2.5V
  - Load current -> 1-~500mA
  - Efficiency > 95%
- Buck_REG2
  - Input supply 3V-> 1.8V
  - Output voltage range -> 0.75V-1.4V
  - Load current -> 1-~250mA
  - Efficiency > 95%
- Buck_REG3
  - Input supply 3V-> 1.8V
  - Output voltage range -> 0.7V-1.4 V
  - Load current -> 0.1-~50mA
  - Efficiency > 95%
- LDO_REG1
  - Input supply 3V-> 1.8V
  - Output voltage range -> 0.6V-1.4V
  - Load current -> 1-~300mA
- LDO_REG2 & 3 (>300mV diff between i/p & o/p)
  - Input supply 3V-> 1.2V Output voltage range ->0.6V-1.4V
  - Load current -> ~10mA (internal cap)

Verification Services

IP Verification Flow



RISC-V based Design and Verification Strategy

Level	Deliverable	Services

Core	• Verified RiscV Core (RTL)
	  • Can add client-specific instructions
	• RiscV SW toolchain
	• OS and drivers
		• Verification of client core (including extensions)
		  • Using random stimulus
		• Architectural compliance
		  • With compliance suites

Subsystem	• Verified subsystem
	  • Single or multiple RiscV Cores
	  • Bus infrastructure
	  • Minimal IP (serial + memory interfaces)
	• Software
	  • Toolchain, OS and drivers
	  • Running on the subsystem
		• RTL Integration
		  • Single or multiple client core(s)
		  • Bus infrastructure
		  • Mix of client and SChipSemi IP
		• Subsystem verification
		• Software
		  • Development or porting of software

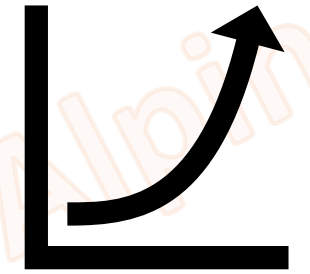
Chip	• HW/SW upport for specific verticals – e.g.
	  • Security IP, hardening, ..
	  • Safety lock step, fault coverage
	  • AI accelerator
		• Full SoC development (RTL to GDSII)
		• Interface with Fab
		• Post-Si test, validation, qualification
		• Product development
		  • Board development
		  • Development or porting of software

SoC Verification Environment

- Testbench Architecture:
  - The testbench for verifying the connectivity between the processor and the peripheral consists of a C environment which mimics the behavior of the software, and an UVM environment for generating the transactions or response from slave/model/endpoint side.
- The C environment:
  1. Typically configures the design for different modes of operation, interrupt settings, speed etc. (controller – SD Host, DDR, Host ; Root Complex – PCIe, Master – I3C, I2C, SPI)
  2. Sets up packets for transmission in DDR or OCM for the Master/Host Controller to read.
  3. Sets up descriptors for the storage of received packets.
  4. Includes ISR routines.
  5. Tests also include self-checkers for checking packets received by software.
- The UVM Environment
  a. Responds to the transactions sent by the master/Host Controller/Root Complex
  b. The UVM environment can be configured to generate random constrained stimulus, with provision for error injection and error detection
  c. Probes are added at the interfaces and interconnects and information collected by monitor is passed to the scoreboard to check the transmitted and received packets/transactions are as expected.
  d. Includes functional coverage groups for individual, cross and sequence coverage

Verification Consultation Service

- Aim for effective, efficient verification
  - Improve quality
  - Reduce costs
  - Improve time-to-market
  - Even under growing complexity



Complexity

The consultation service offers

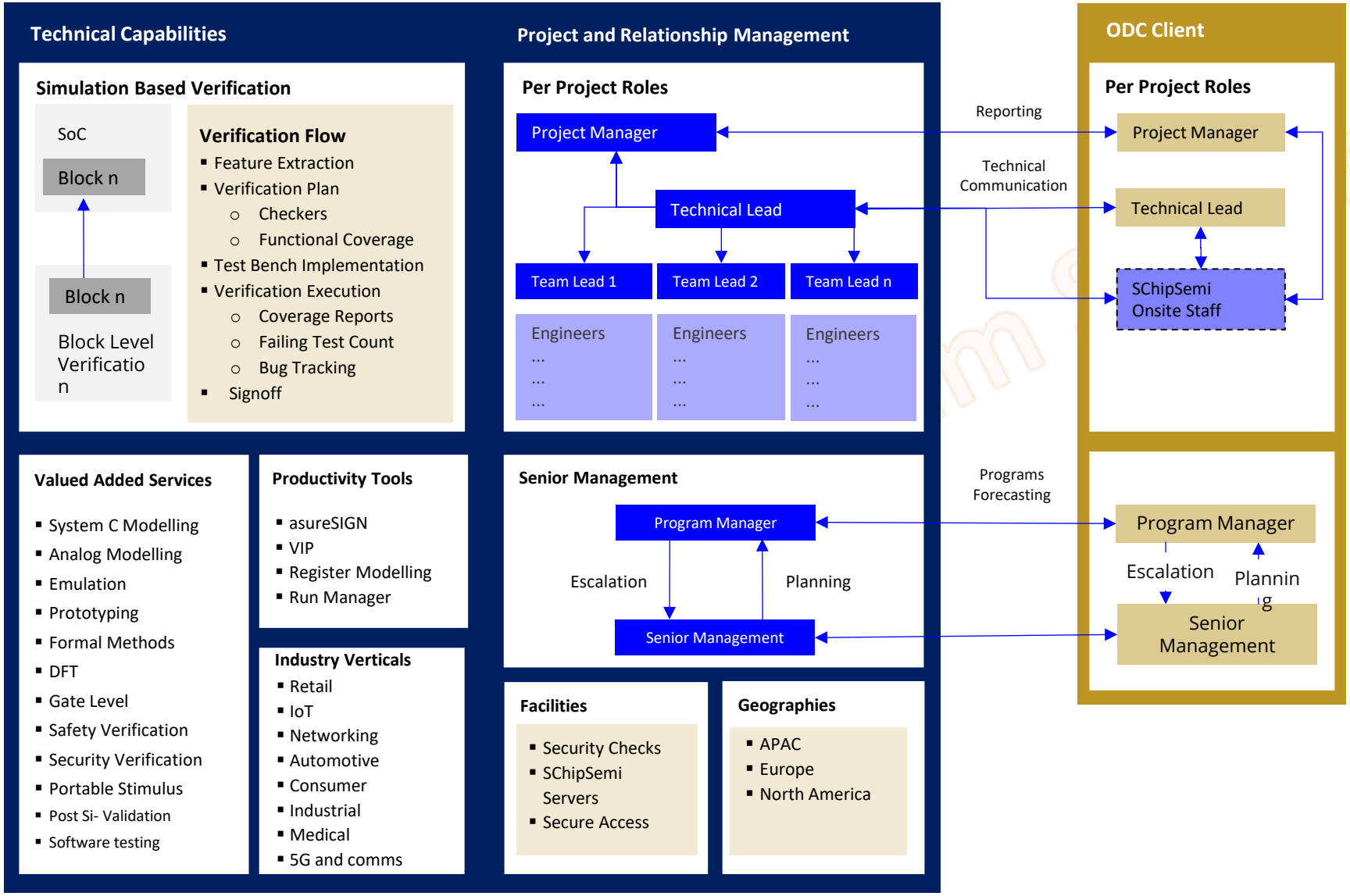
- A full review of current methodologies
- Prioritized list of improvement suggestions
- Pilot projects to trial those improvements
  - E.g. SV-UVM at IP and SoC
- A full roll out program
  - Well defined targets and milestones
  - Full use of metrics and dashboards
  - Training of engineers and managers
  - Execution services to help ramp-up

We ensure that at the end of the rollout, that your organization can continue standalone

- But we offer continued support

This service has been successfully implemented in more than 10 clients

Verification ODC Capabilities



Advantages

- Build expertise in team
  - Retain team
- Value add services
- Run multiple projects in parallel
- Expand teams quickly
  - Cope with growth
  - Can also shrink team

Dr. Michael George Bartley

Mike Bartley
Founder and CEO

Dr. Mike Bartley has over 30 years of experience in software testing and hardware verification, having built and managed advanced test teams at companies like STMicroelectronics, Infineon, Panasonic, and ClearSpeed. He has also advised organizations such as ARM, NXP, and startups on verification strategies.

A pioneer in applying artificial intelligence (AI), Mike began using genetic algorithms in 1998 and now helps businesses integrate AI to enhance efficiency and customer engagement.

Mike founded a software test and hardware verification services company that grew to 450+ engineers, serving over 50 clients globally. This company was acquired by Tessolve Semiconductors, where Mike was Senior VP. He focused on integrating the latest verification and AI techniques in VLSI projects and leads Tessolve's Centres of Excellence, which include AI R&D initiatives.

He holds a **PhD in Mathematics** from Bristol University, along with **nine MScs** in fields such as software engineering, AI, and blockchain. Mike is also studying quantum computing and technology in healthcare. He is the Board Advisor and Technical Team Head of **Suresh Chips and Semiconductor Private Limited.**

Thank You!

CONTACT US TODAY:

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