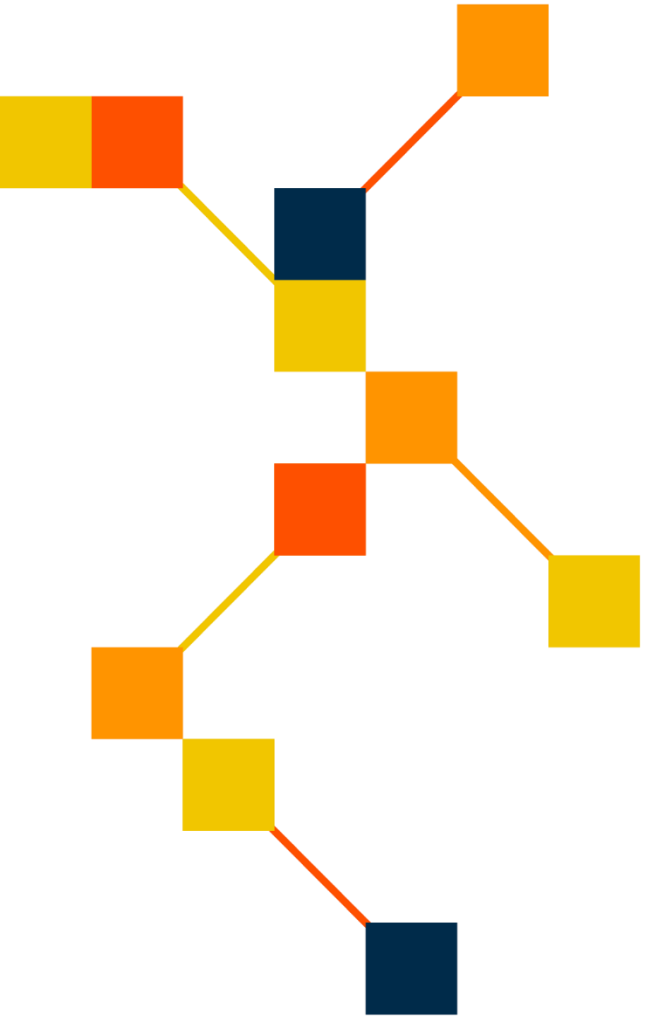


NoC Automation

How smart NoC IP prevents sub-optimal network-on-chip implementations that DV tools cannot catch

Rick Bye, Director Product Management

23rd September 2025

ARTERIS IP

Who is Arteris? – The Leading Semiconductor System IP Company

Global customer base producing billions of SoCs

System IP Leader

- Founded in 2004; QCOM M&A 2013; Re-established in 2014
- Pioneers of Network-on-Chip (NoC) IP
- October 2021 IPO (Nasdaq: AIP)
- Global Team of 250+ employees
- 94 patents issued, 120 applications
- ISO 9001:2015 and ISO 26262 Certified

Proven Customer Successes

- 3.7B+ SoCs shipped in electronic systems
- 200+ active customers
- 850+ SoC design starts
- Used by 9 out of the top 10 semiconductor companies
- 90%+ customer retention rate
- Ecosystem: Any processor, any IP, any EDA, and any Foundry

Connected with the Ecosystem

Diversified Customer Base

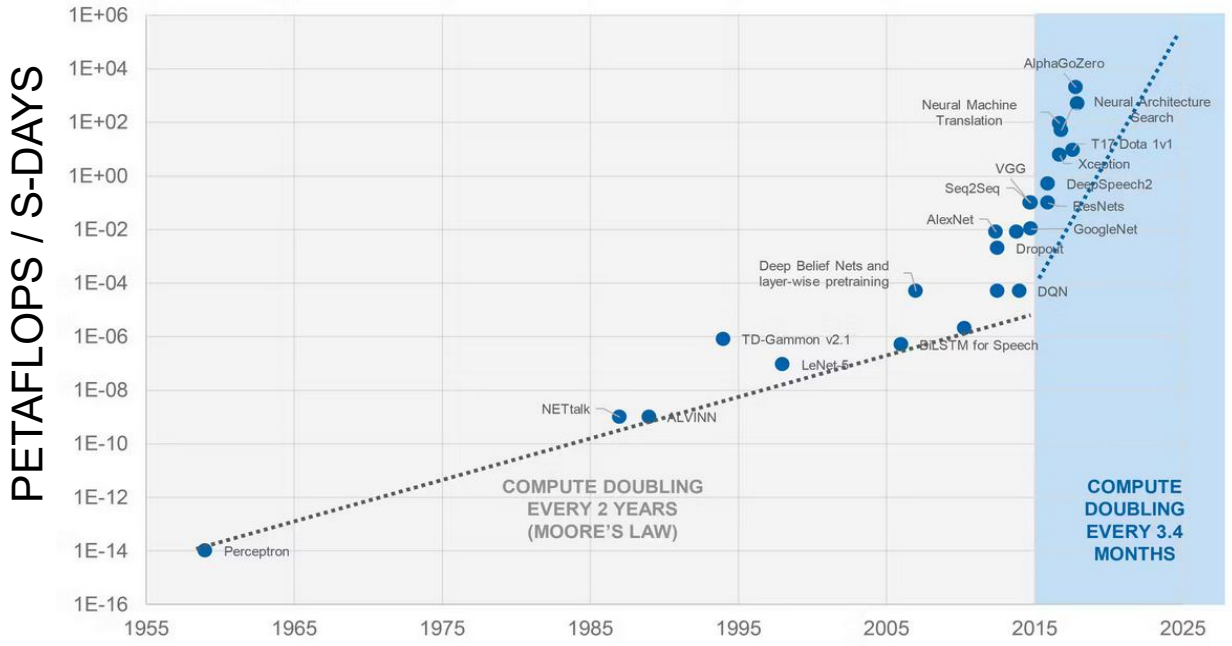
Subset of Publicly Disclosed Customers

Global Customer Support

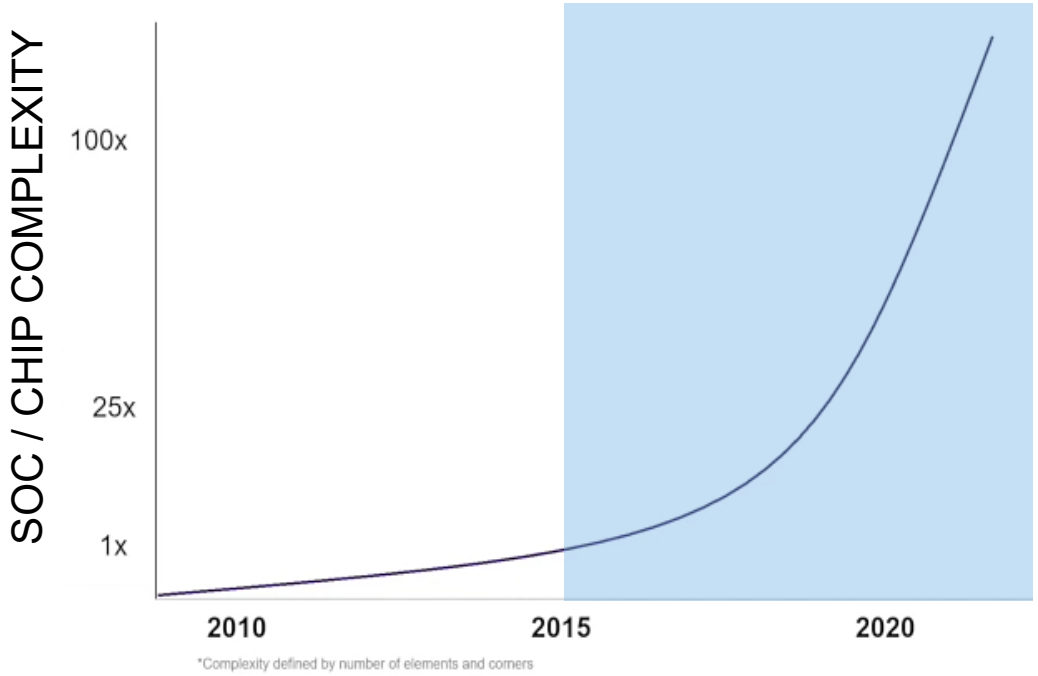
Moore’s Law is history…

AI Demands are Accelerating the Rise in Chip Complexity

AI Era of Compute: 7X Acceleration



Driving Exponential Chip Complexity

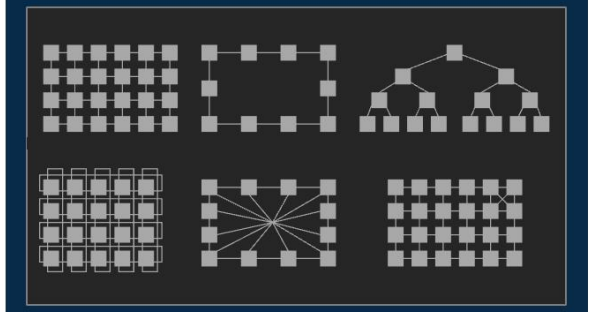


Modern silicon chips are connected by **billions of wires**, ever-expanding with growing complexity
→ **more & bigger networks-on-chip, with more complex architecture / topology setup**

Sources: OpenAI: AI and Compute Research Report, Semi Engineering, Synopsys

High Performance SoC Market Trends and Challenges

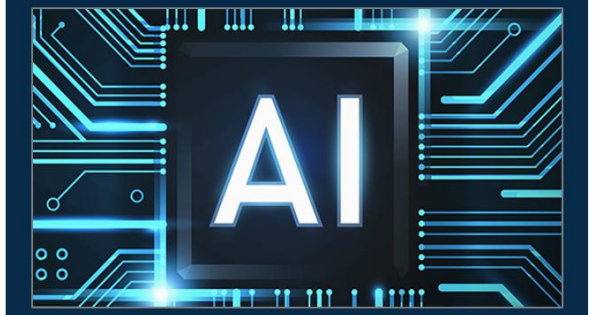
Accelerating Complexity



More Processors & IP Blocks Data movement key competency ‘Data movement and storage operations can account for up to 84% of the dynamic energy usage of a GPU's system-on-chip (SoC)*.’

*Source: HAL open science paper, Jun’24

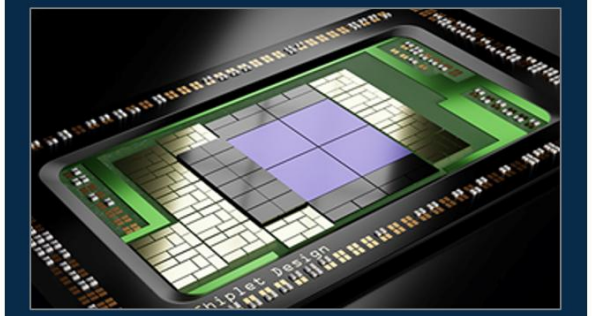
Artificial Intelligence



By 2030, the total generative AI compute will serve 70 percent of business-to-consumer and 30 percent of business-to-business applications **.’

**Source: McKinsey, Mar’24

Chiplets



‘Multi-die systems have emerged as the solution to go beyond Moore’s law and address the challenges of systemic complexity***.’

***Source: Semiconductor Engineering Oct’23

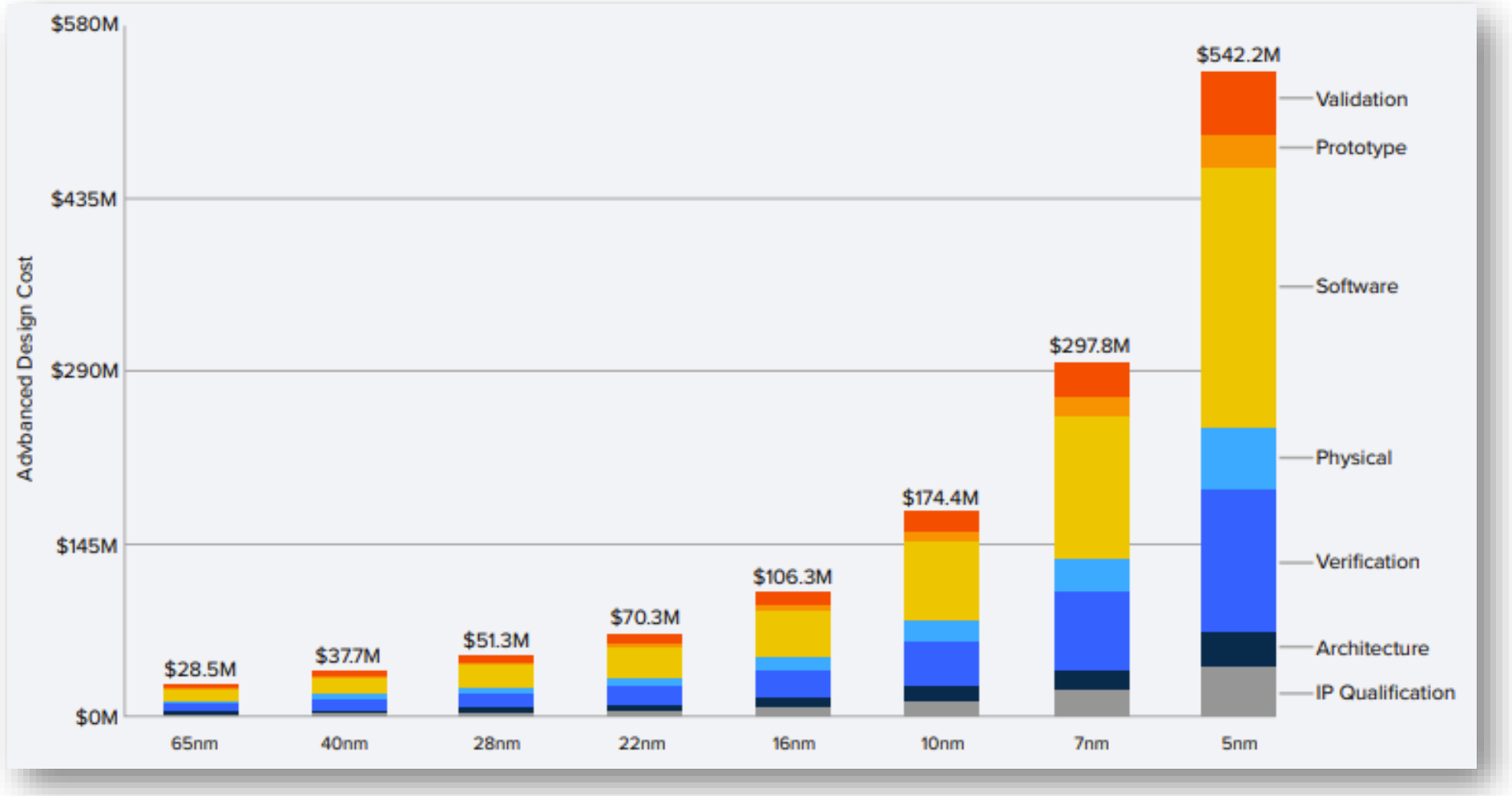
OEMs Going Vertical

‘OEMs are increasingly embracing vertical integration in their design practices, including implementing their own SoCs.****.’

****Source: Synopsys Feb’22

Developing Complex SoCs is Expensive

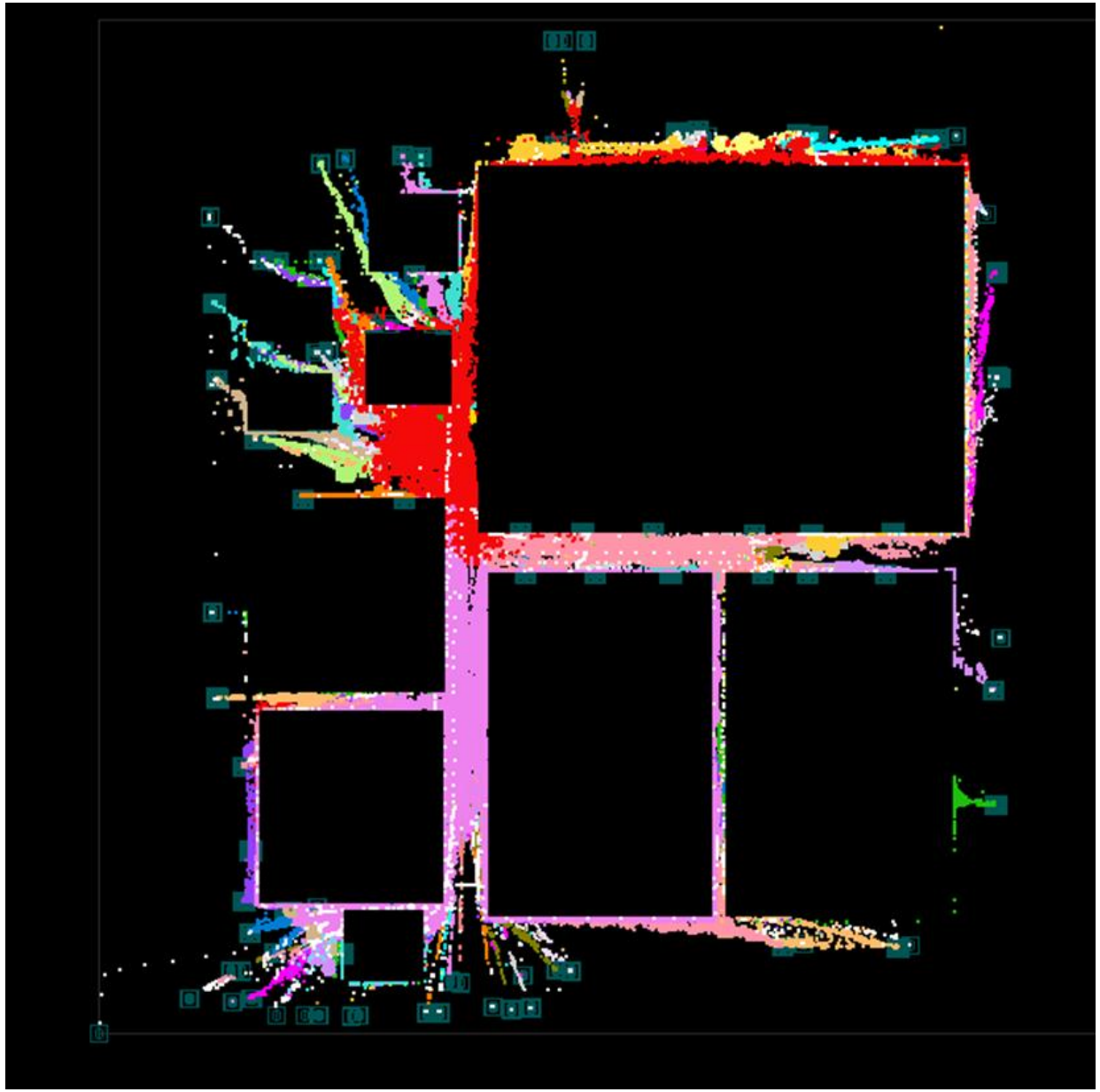
Efficiencies are Critical to Cost Control

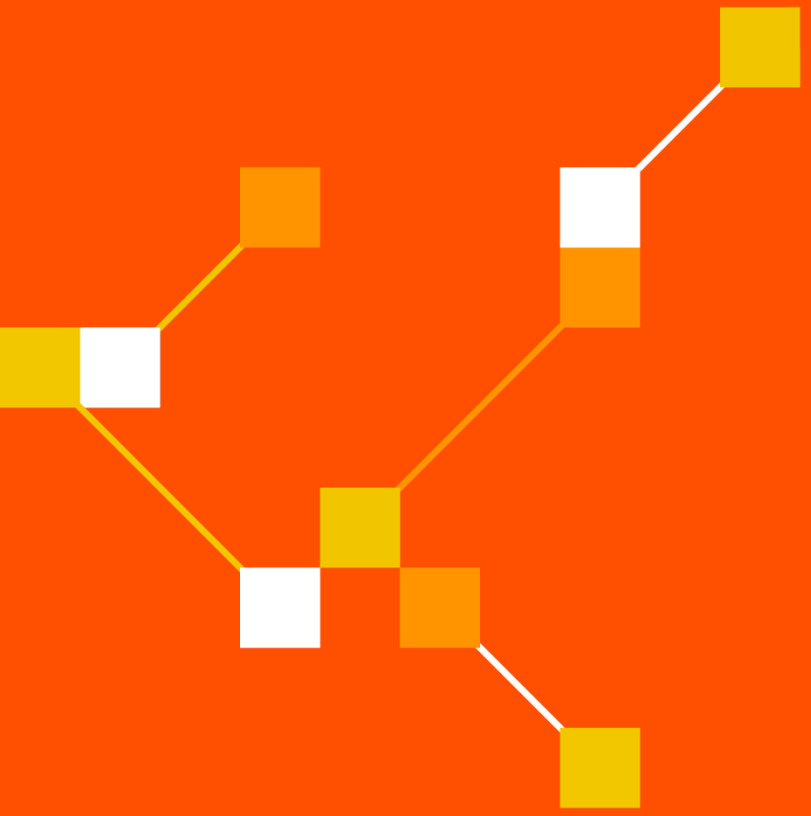


Source: IBS

… except for system IP

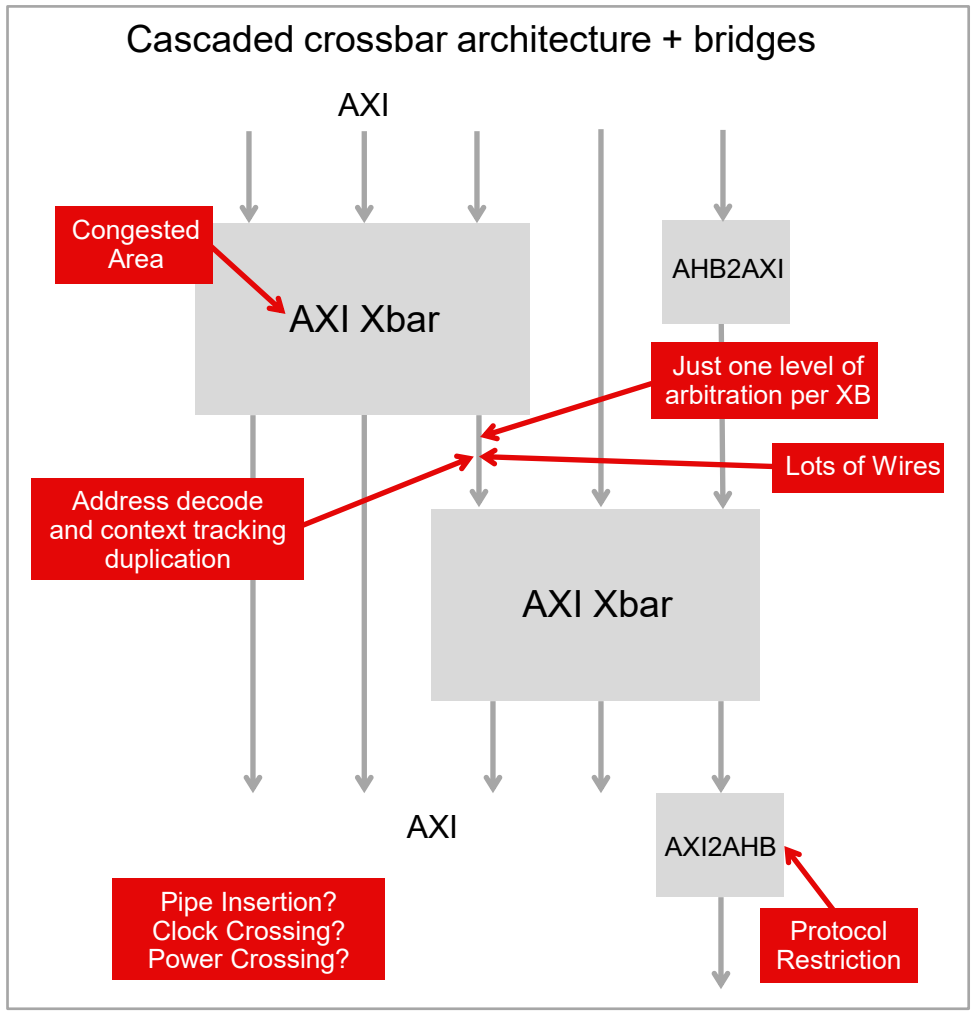
- Interconnect or Network-on-Chip (NoC)
- The framework or chassis that holds the IP together

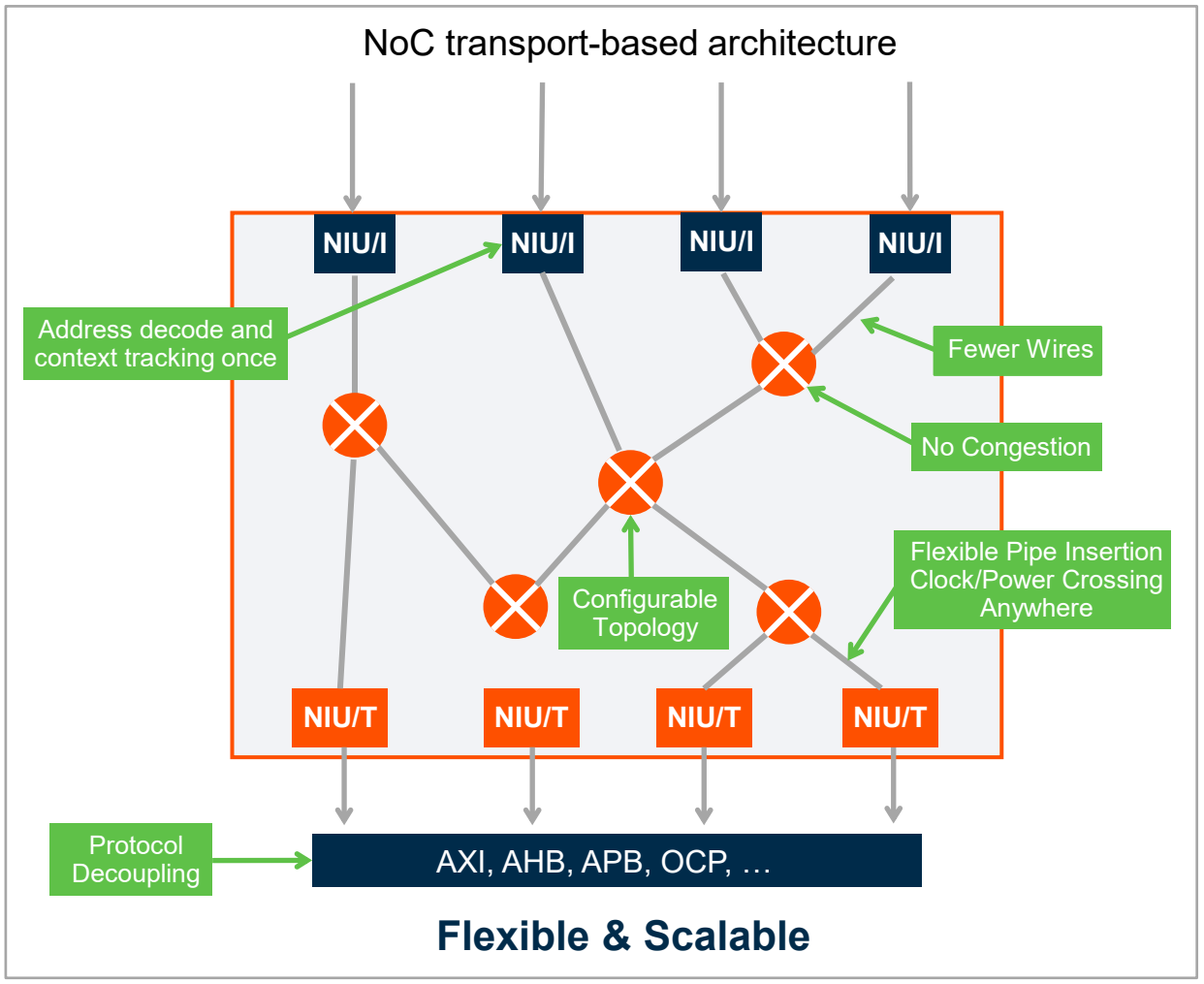




Why a NoC?

NoC technology is better than cascaded crossbars

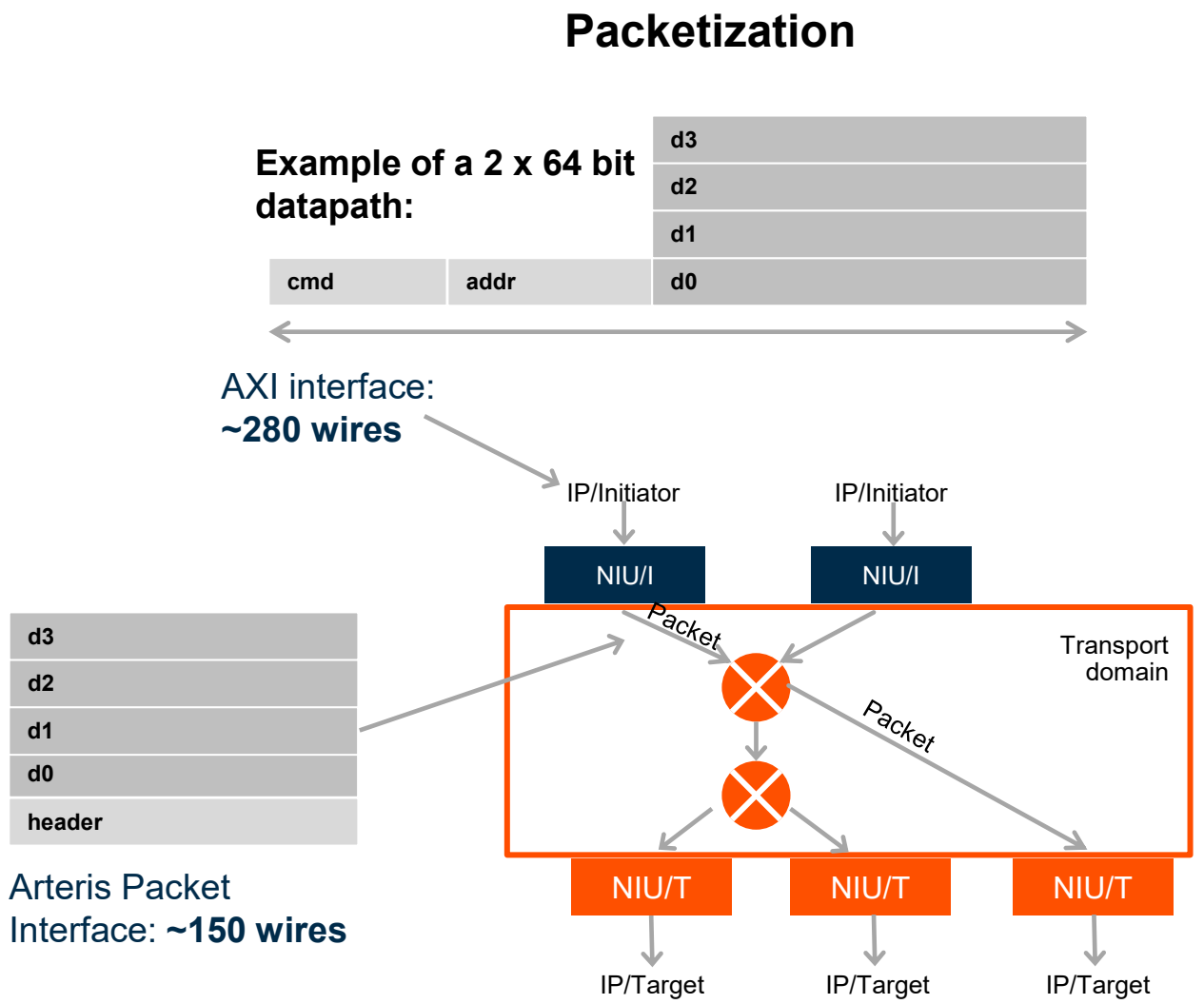




ARTERIS IP

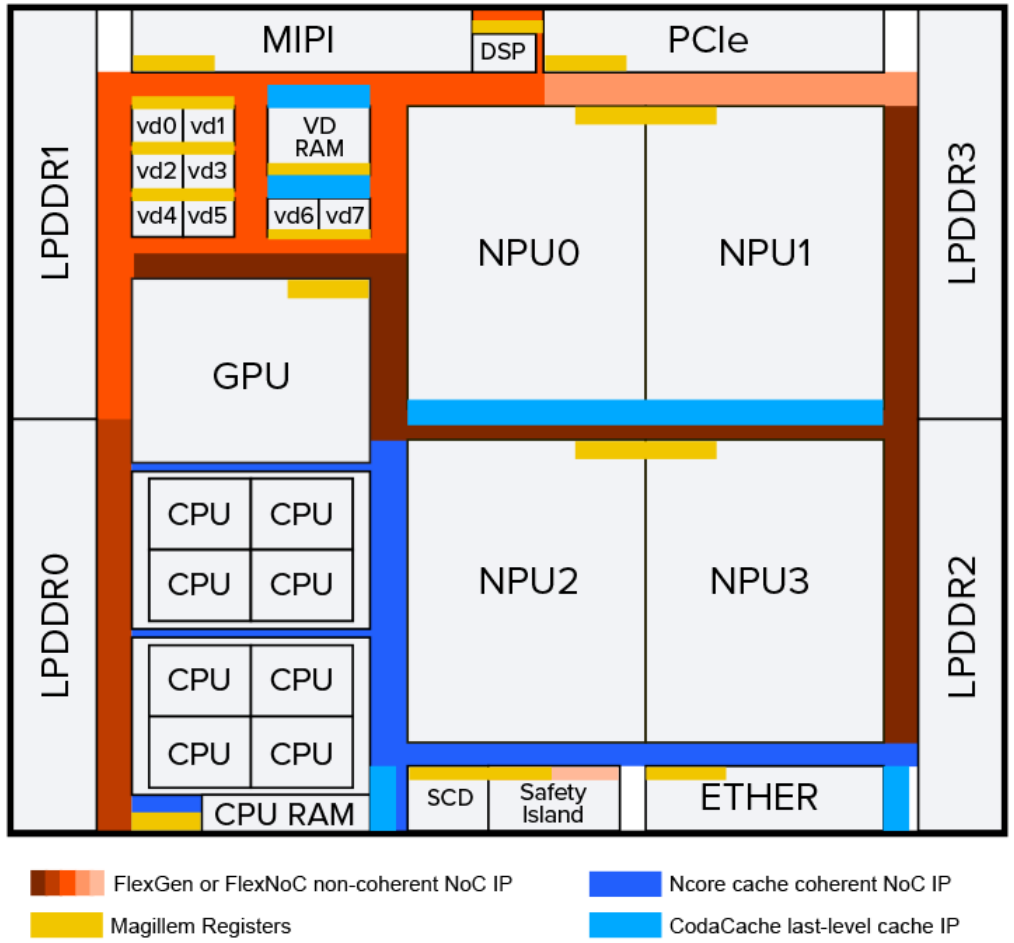
NoCs Packetize data to reduce wires, lowering power consumption

- Reduce routing congestion
  - Packetization – fewer wires
- Ease timing closure
  - Fine grain pipeline stage insertion
- Reduce die area
  - Simpler datapath logic
- Reduce active power
  - Unit-level dynamic clock gating
- Decouple sockets from transport
  - Easier integration



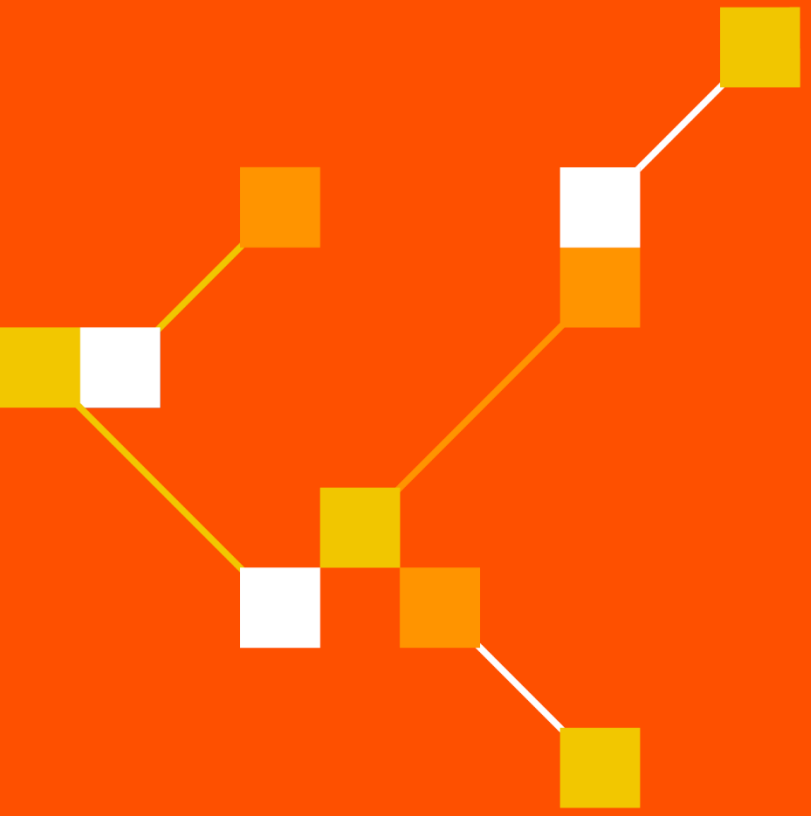
Modern SoCs Require Multiple NoCs For Optimal Performance

5-20 NoCs per chip or chiplet with NoCs representing 10-13% of silicon



NoC Design Challenges

- NoC IP is highly configurable and complex
- Scarce availability of NoC design expertise
- Manual NoC implementation is tedious and prone to errors that DV tools cannot catch
  - E.g. Wires not taking the shortest path
    - Increases area, power and latency
  - Last minute design changes add to risk
- Designers don't try different configurations because a NoC design takes hours or days !



Arteris Smart NoC Technology

Overview

Solution – Smart NoC IP (Arteris' FlexGen)

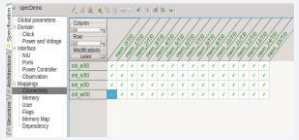
Start and finish physical layout sooner for reduced project cycles and faster time to market without a NoC expert

User Inputs

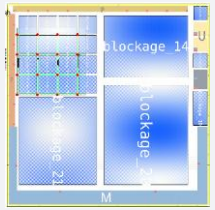
IP socket specifications

	Protocol	wData	wAddr	wID
M1	AXI-4	128	44	8
M2	AXI-3	64	32	4
M3	AHB	32	32	0

Connectivity specifications

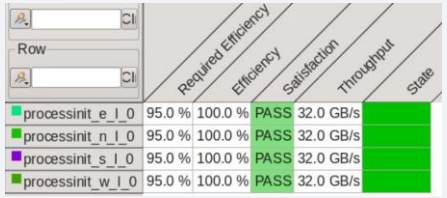


SoC floorplan constraints



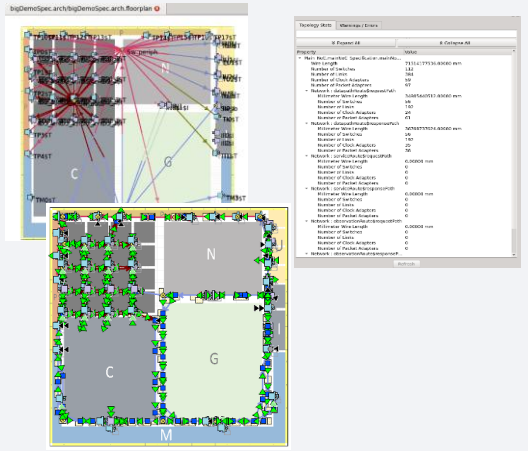
NoC Objectives

Traffic classes specify performance goals for data traffic

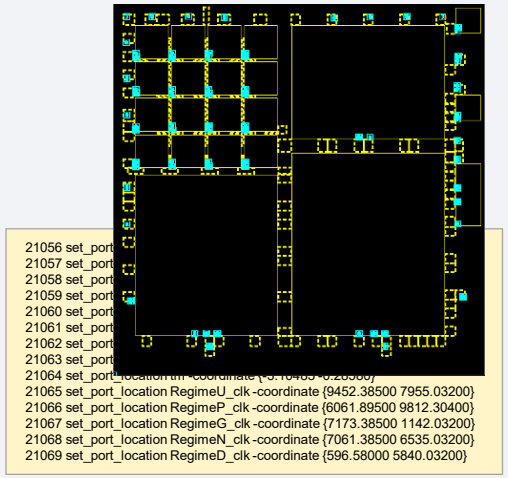


Physically & Performance Aware NoC IP Topology

The smart NoC automatically creates its topology based on the SoC floorplan

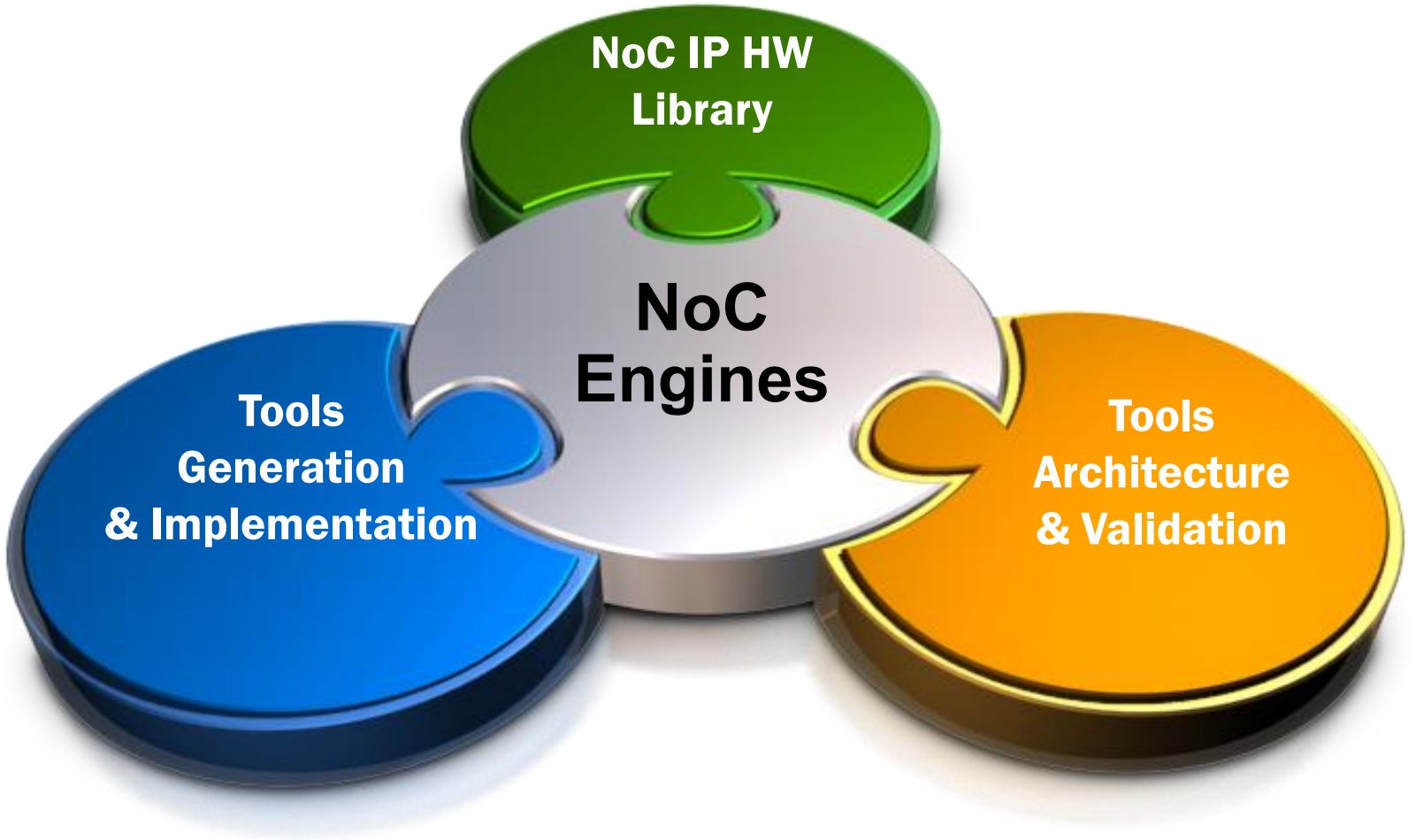


Physical Synthesis Output



Manual NoC Configuration	1 hr-1d	1-2 hrs	1-10days+	<1hr
Smart NoC	1 hr-1d	1-2 hrs	<1 day+ <1 hr	Physical Implementation flow starts earlier when using a smart NoC

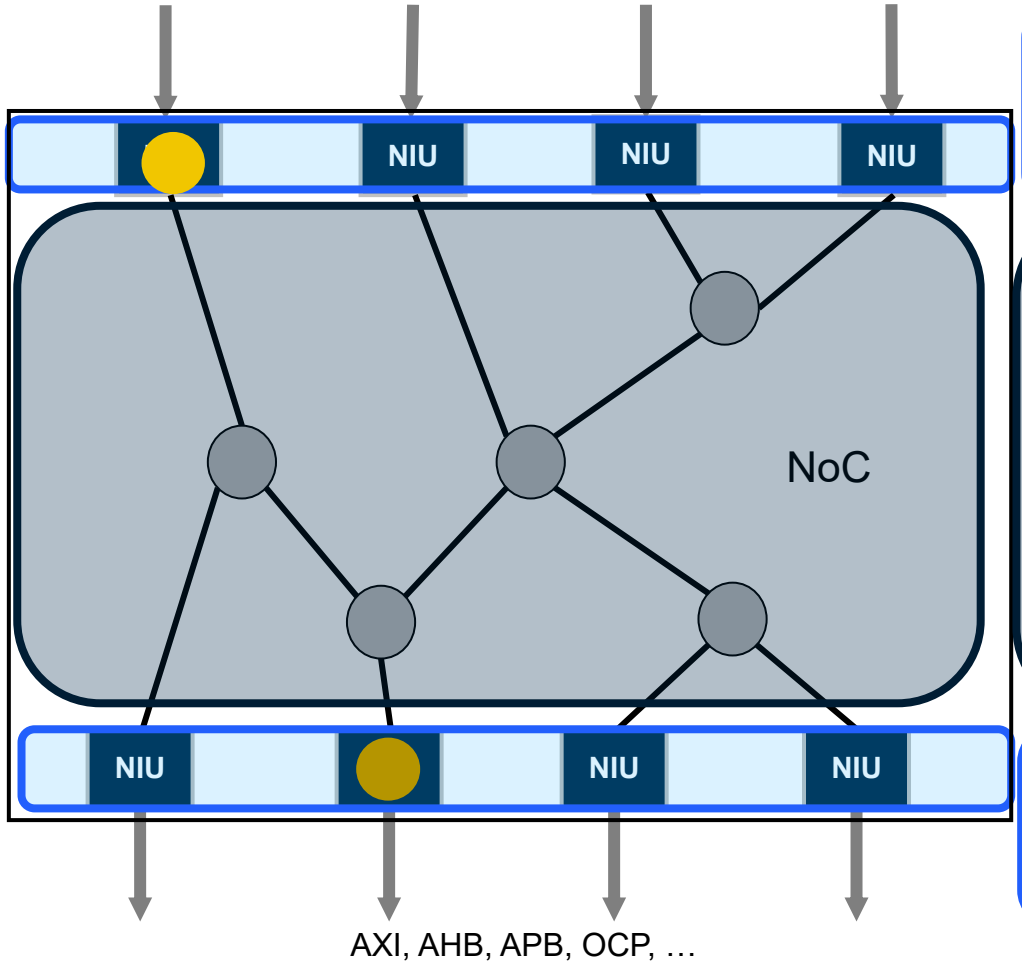
Smart NoC Solution

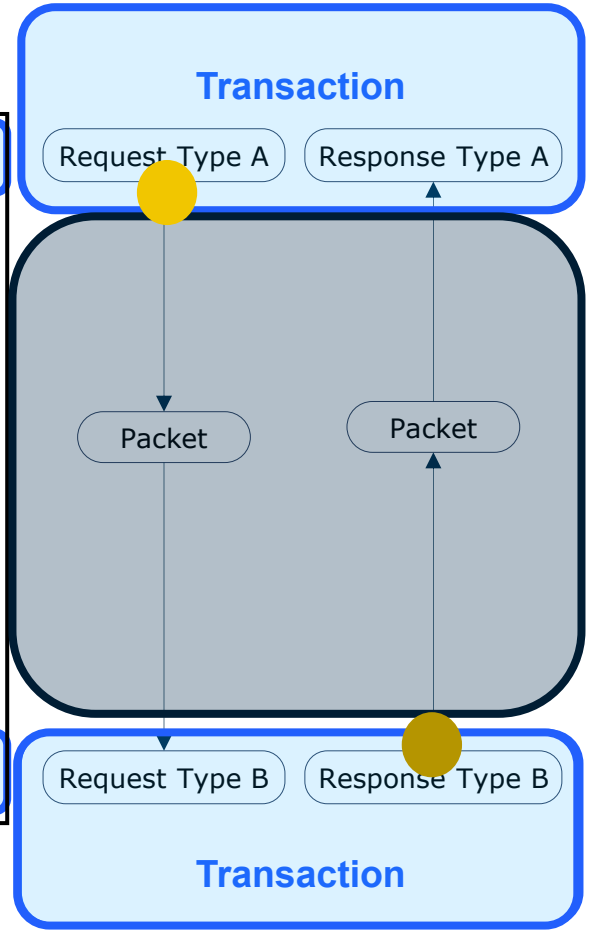


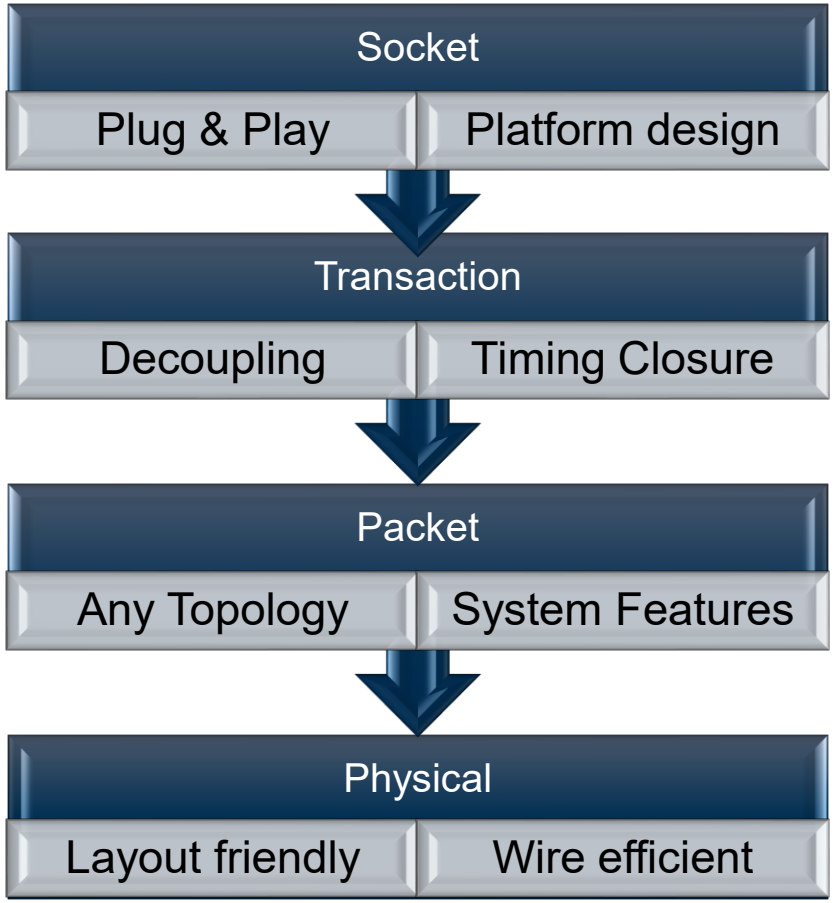
… Layered Approach to Network on Chip Design

Layered architecture

AXI, AHB, APB, OCP, …





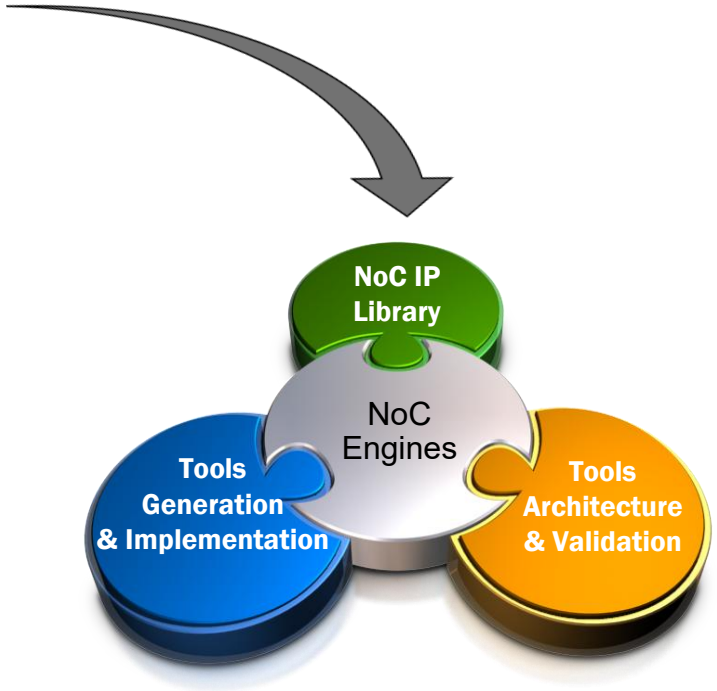


ARTERIS IP

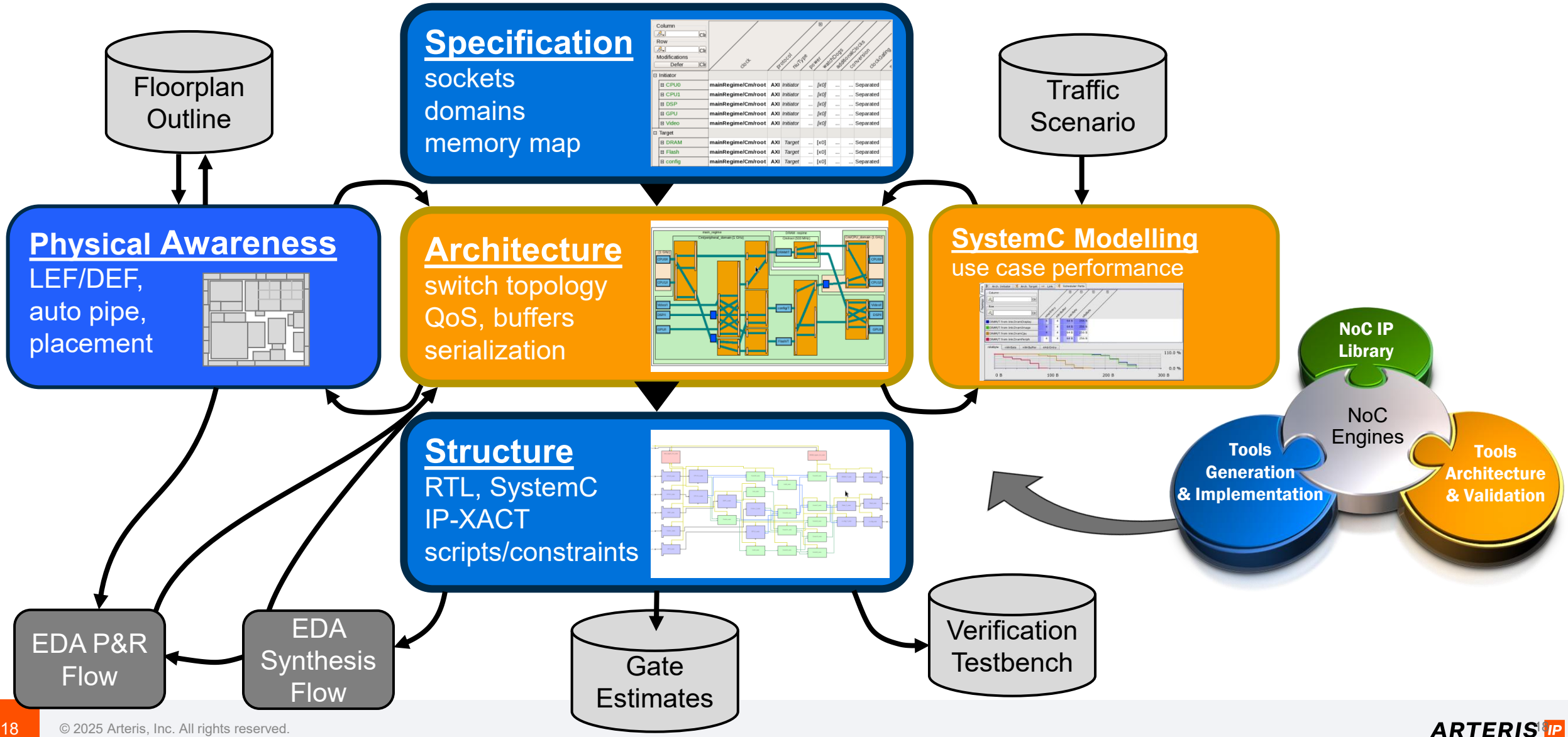
… Built on a Mature IP Library of Small IP Building Blocks

For flexible and scalable designs

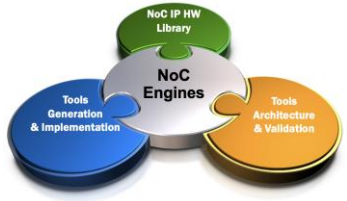
IP Biulding Blocks	Functions
NIU (Network Interface Units)	ACE-Lite, AXI, AHB, APB, PIF, OCP, others
Transport	mux, demux, serializer, buffer
Domain adapter	sync/async clock, power, voltage
Pipeline stage	close timing
QoS	dynamic priorities, bandwidth limiter/regulator
Re-order Buffer	manager for out-of-order memory responses
Security	user defined firewalls
Debug	error, statistics, trace probes
Resilience/Safety Logic	timeout, safety controller, checkers



…Specify, Architect, Generate and Verify Methodology



Smart NoC Technologies



Designer input

Constraints
Interfaces
Memory Map
Safety
Floorplan

Intent
Perf & QoS
Domain
Debug
Security

NoC Tools

Capture
Constraints & Intent

User Interface
Back annotation

Collateral export

NoC Engines

Generation
Topology creation

Timing solving
Pipeline insertion

Assembly
Parameters resolution

Estimation
Timing & Area

Creation
Verilog & SV & Doc

NoC Libraries

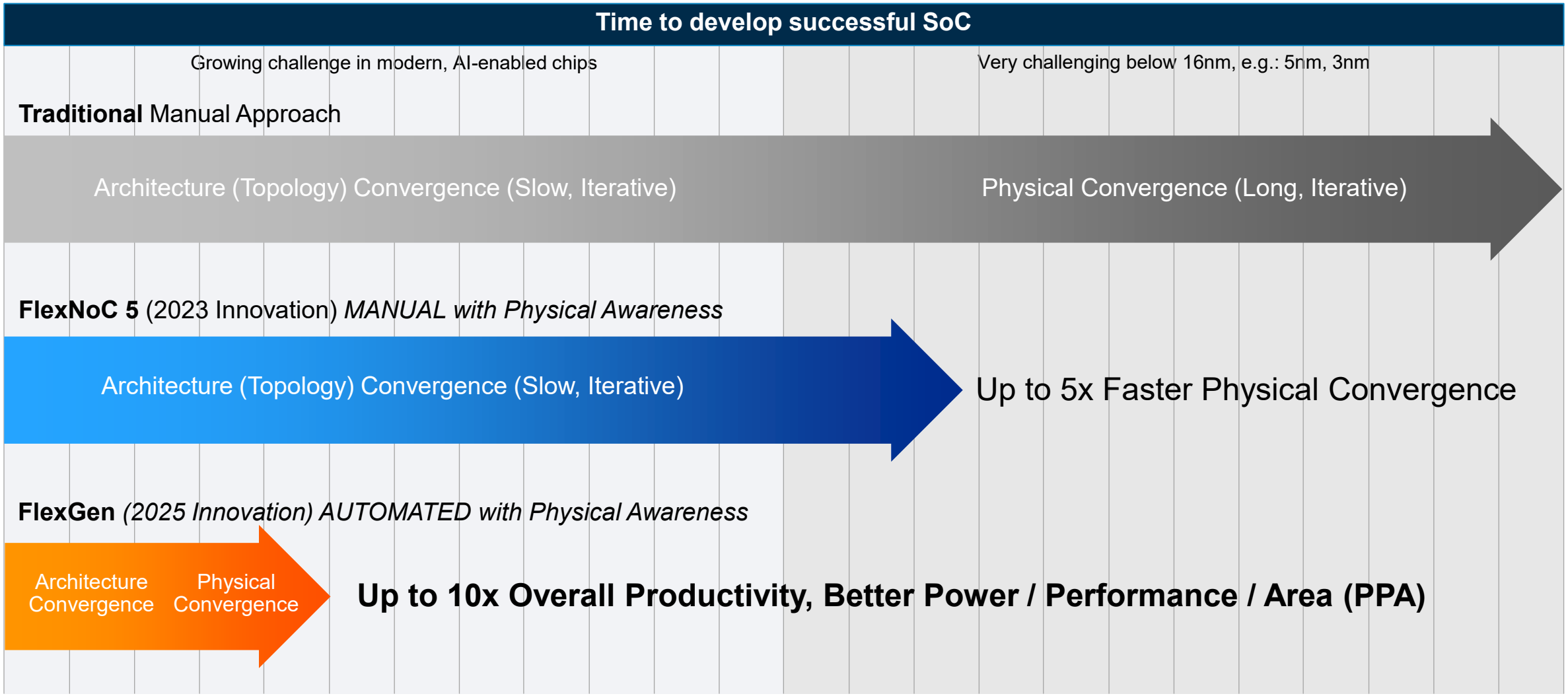
NoC System IP Library
NoC IP Library
Protocols

Foundation library

ARTERIS IP

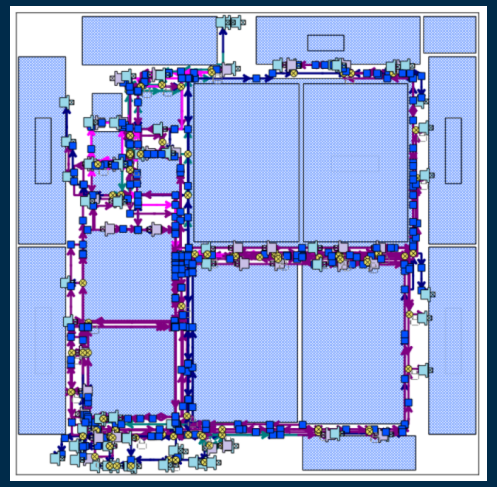
Arteris' FlexGen Builds on FlexNoC's Physical Awareness

Network-on-chip technology – manual and automated – at the heart of tomorrow's chips



FlexGen - Smart NoC IP Example of Performance and Efficiency Advantages

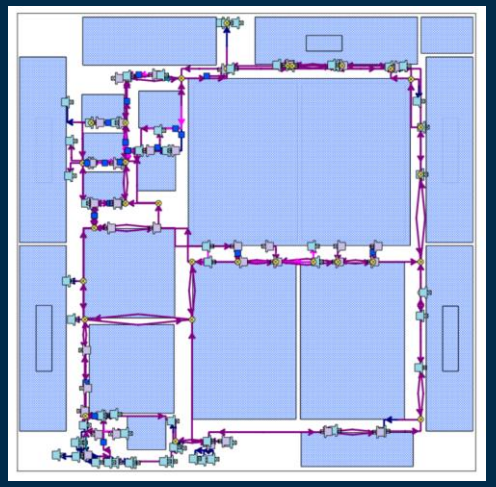
Manual with best effort performance



FlexNoC

Wire length: **313.0 m**

Automatic with wire length focus

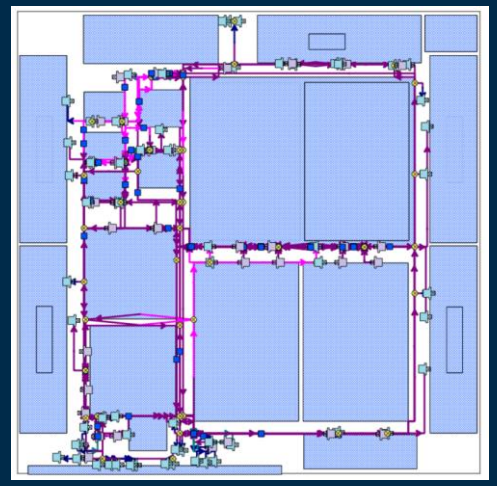


FlexGen

Wire length: **116.0 m**

Performance for greater efficiency including more bandwidth and less latency

Automatic with all performance goals



FlexGen

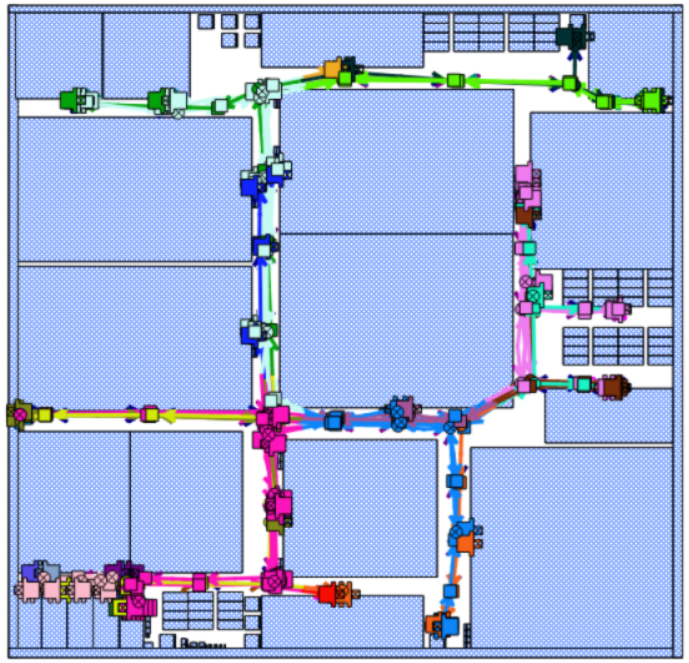
Wire length: **280.8 m**

Advantages: reduced wire length, lowered power consumption and minimized congestion

Sample Results for Automotive AI SoC (ADAS)

DREAM CHIP

Manual



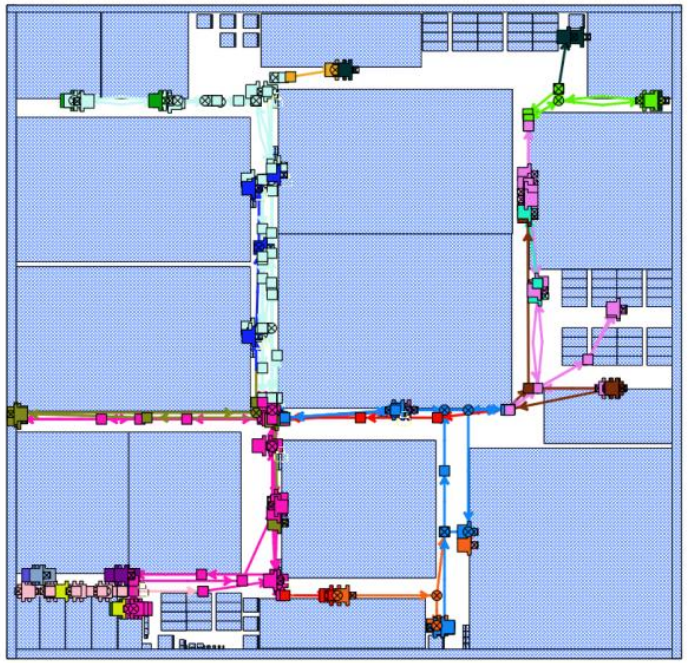
Total Wire Length	138,709 mm
Length of Longest Wire	904 mm
Number of Switches	258
Number of Links	313
No. of Clock Adapters	152
No. Packet Adapters	157
Latency	65.18 ns
Maximum Latency	1005.67 ns
Main NoC area	3.64 mm^2

10x productivity
-26% wire length
-28% longest wire

-5% latency
-51% max latency
-3% area

Source: Dream Chip Technologies

Smart NoC Automated

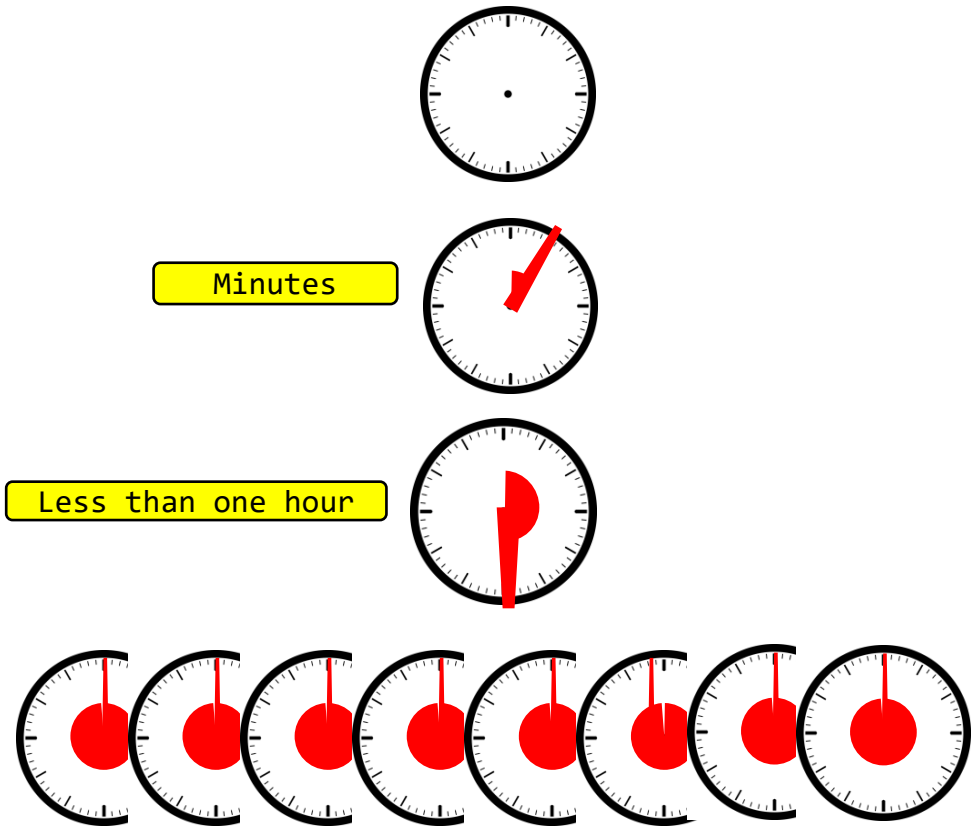


Total Wire Length	102,587 mm
Length of Longest Wire	650 mm
Number of Switches	282
Number of Links	420
No. of Clock Adapters	141
No. Packet Adapters	210
Latency	62.08 ns
Maximum Latency	491.67 ns
Main NoC area	3.51 mm^2

ARTERIS IP

FlexGen: Reduced Turnaround Compared To Manual NoC Generation

Incremental change turn-around time



Smart NoC Flow (Arteris FlexGen)

Step 1
- Create a Network-on-Chip **specification**
- Assign initial high-level performance parameters
- **Verify performance** with architectural model and simulation

Step 2
- Capture virtual **floor planning** constraints and specify **performance intent**
- **Smart NoC** generates Network-on-Chip topology
- **Verify performance** with architectural model and simulation

Step 3
- Insert **pipeline** slice with built in Static Timing Analysis (STA) engine
- **Verify performance** with architectural model and simulation

Step 4
- Create a physical synthesis **framework**
- Validate with physical synthesis tools using Smart NoC **constraints**

Smart NoC IP Summary

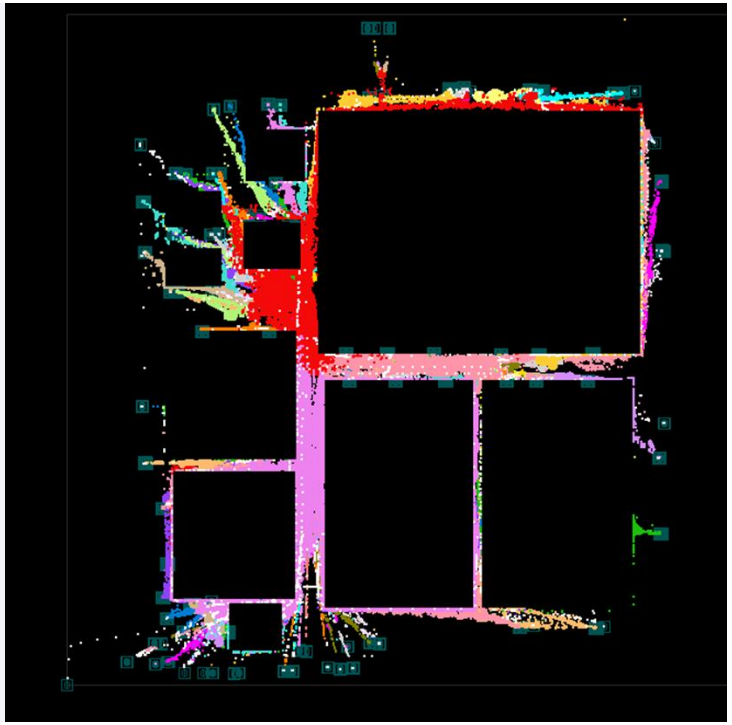
Arteris Revolutionizes Semiconductor Design with FlexGen - Smart Network-on-Chip IP NoC Automation Delivers Productivity Improvements and Better Quality of Results

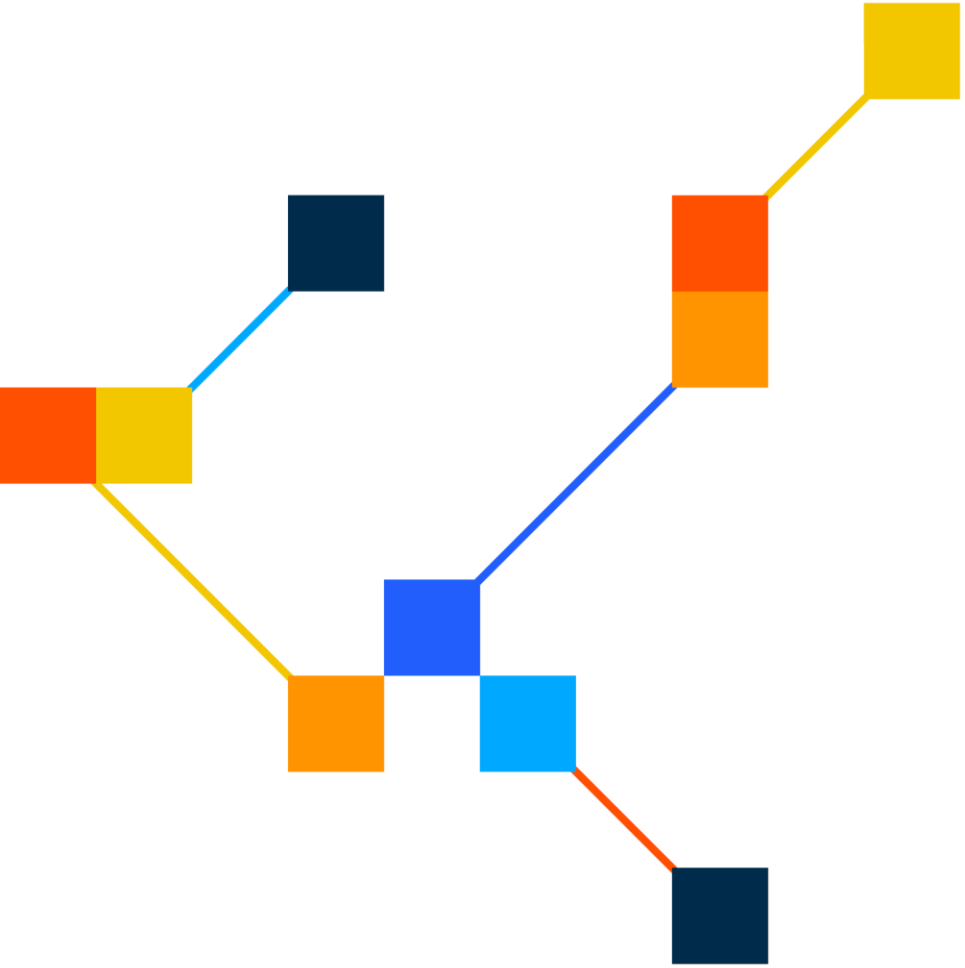
Challenge:
SoC design complexity has surpassed manual human capabilities, requiring smart NoC automation.

Smart NoC IP from Arteris delivers:

- **Productivity Boost:** Accelerates chip design by up to **10x**, shortening and reducing iterations from weeks to days for greater efficiency.
- **Expert-Level Results:** Enhances engineering efficiency by **3x** while delivering expert-quality results with optimized routing and reduced congestion.
- **Wire Length Reduction:** AI-driven heuristics reduce wire length by up to **30%**, improving chip or chiplet power efficiency.

Connects any processor (Arm, RISC-V, x86) and supports industry protocols.





ARTERIS IP

Thank You

For additional information contact
info@arteris.com