SYNOPSYS®

Hardware Emulation for HW-SW Co-Verification of Heterogeneous SoCs

Jean-Philippe Binois – Sr Director Application

Sep. 2025

Legal Disclosure

CONFIDENTIAL INFORMATION

The information contained in this presentation is the confidential and proprietary information of Synopsys. You are not permitted to disseminate or use any of the information provided to you in this presentation outside of Synopsys without prior written authorization.

IMPORTANT NOTICE

This presentation may include information related to Synopsys' future product or business plans. Such plans are as of the date of this presentation and subject to change. Synopsys is not obligated to update this presentation or develop the products with the features and/or functionality discussed in this presentation. Additionally, Synopsys' products and services may only be offered and purchased pursuant to an authorized quote and purchase order or a mutually agreed upon written contract.

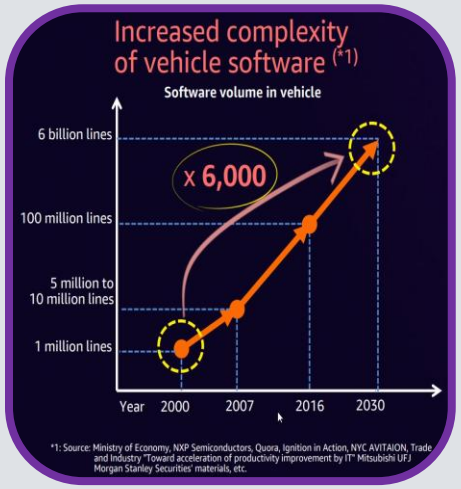
FORWARD LOOKING STATEMENTS

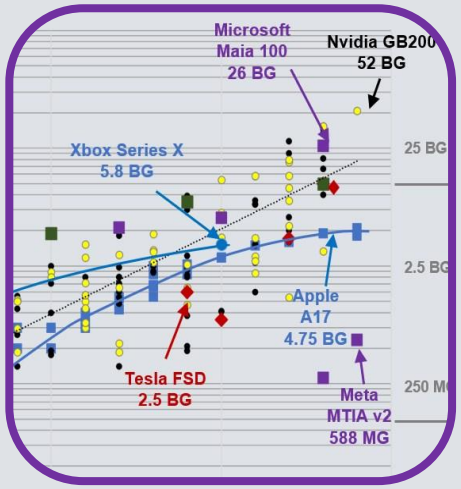
This presentation may include certain statements including, but not limited to, Synopsys' financial targets, expectations and objectives; business and market outlook, business opportunities, strategies and technological trends; and more. These statements are made only as of the date hereof and subject to change. Actual results or events could differ materially from those anticipated in such statements due to a number of factors. Synopsys undertakes no duty to, and does not intend to, update any statement in this presentation, whether as a result of new information, future events or otherwise, unless required by law.

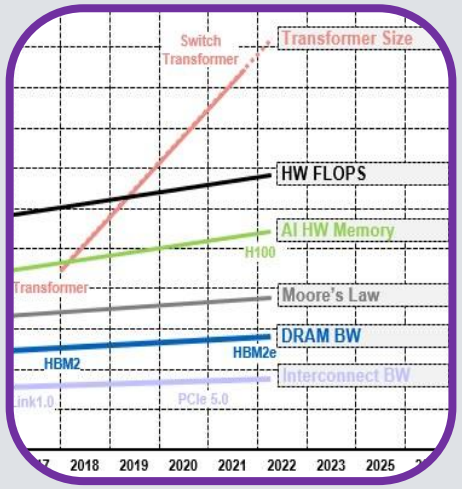
Compounding Complexities

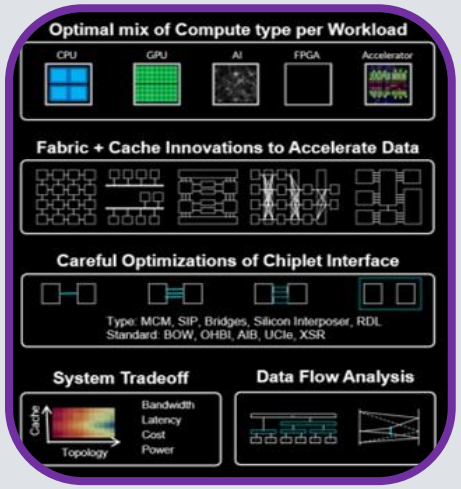
Hardware-assisted Verification (HAV): The **keystone** for ensuring functionality, power and performance

Software × **Hardware** × **Interfaces** × **Architectures**









Verification Challenge: **Quadrillions of Cycles***

Sources: AWS, Synopsys, AI and Memory Wall: 2403.14123 (arxiv.org), Baya Systems, *"What Makes RISC-V Verification Unique?" https://bit.ly/4hDXCe9

Verification Happens in Phases – **Quadrillions of Cycles!**

From ISA Through CPU, Clusters of CPUs and Systems on Chips / of Chiplets

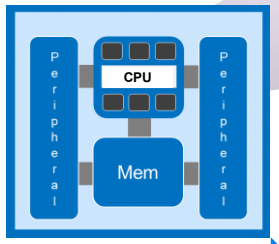
Simulation 10s Hz

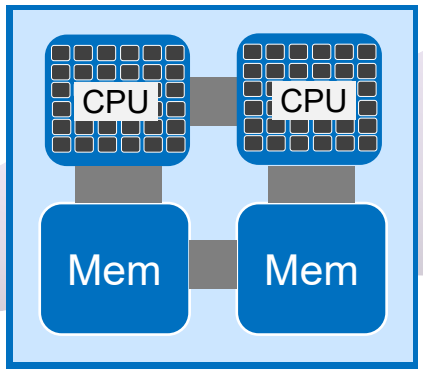
Silicon At Speed

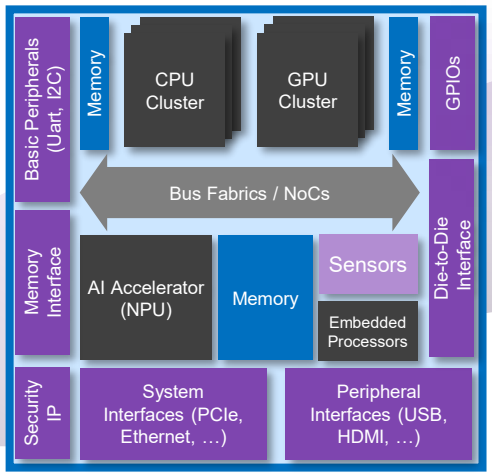
Hardware Assisted Verification (HAV)

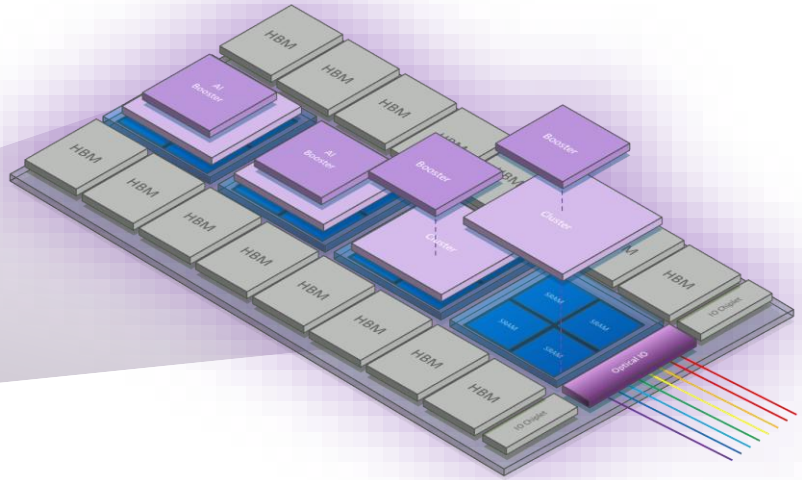
Example average per CPU IP*:

- 5-6 Trillion cycles (in emulation)
- 2-3 Peta cycles (in prototyping)







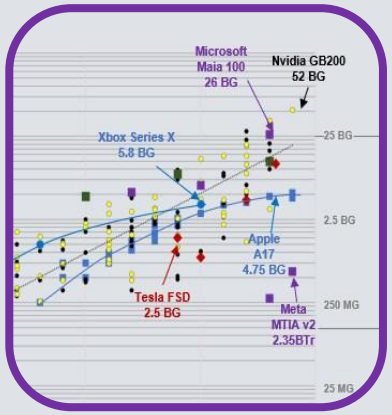


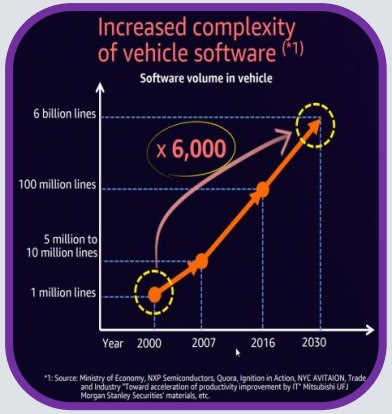
IP/Core Centric → **Subsystem / Software** → **Full Chip(let) / Software** → **Multi-die / Software**

*"System Validation at ARM: Enabling our Partners to Build Better Systems", https://bit.ly/3WLCvhr, https://bit.ly/3CEMBd0

Synopsys Leads Industry Delivering HAV Innovation

Hardware



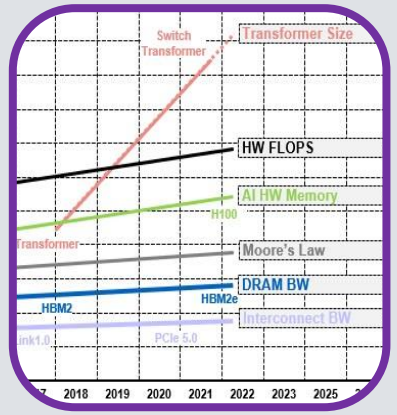


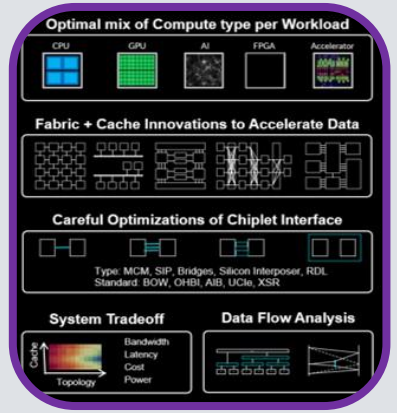
Software

HAV Platforms

- Performance
- Scalability
- Total cost of ownership
- Configurability

Interfaces





Architectures

Sources: AWS, Synopsys, AI and Memory Wall: 2403.14123 (arxiv.org), Baya Systems,

Synopsys HAV Product Family

Highest Scalability, **Best Density**

NEW

HAPS-200 & ZeBu-200

Highest Performance, **EP-Ready Hardware**

Extended

EP-Ready Hardware

AMD Partnering with Synopsys

"The future of emulation and prototyping demands unprecedented **performance**, **adaptability**, and **scalability.”**

By **integrating** the **AMD Versal Premium VP1902 adaptive SoC**, with its industry-leading capacity*, performance, and debug capabilities, into **Synopsys' EP-Ready platforms** we're not only improving **performance metrics**, we're also transforming how engineering teams can validate and optimize their most ambitious new ASIC and SoC designs. Our **longstanding partnership with Synopsys** empowers design teams to tackle their most complex verification challenges, from **AI/ML workloads** to **multi-die architectures**, while dramatically **accelerating time to market**.”

Salil Raje
Senior Vice President and General Manager
Adaptive and Embedded Computing Group at AMD

**Based on AMD internal analysis in May 2023 with a 6-input LUT count to compare the Versal Premium VP1902 device versus competitor offerings*

Synopsys HAV Product Family

Highest-performance and Most Versatile HAV Systems

ZeBu

ZeBu Server 5

Highest Capacity-Scalable Emulation Platform
(>60BG with Modular HAV Methodology)

New: ZeBu-200
ZeBu EP1/EP2

Highest Performance Emulation Platform
(up to 15.4 BG)

EP-Ready HW

EP SW Transition

HAPS

New: HAPS-200
HAPS-100 4F/12F

Highest Performance Prototyping Platform
(Up to 10.8 BG)

HAPS-100 1F

IP Prototyping Platform
(<100 MG)

Hardware-Assisted Verification Solutions

HAV Product Portfolio supporting Synopsys IP Protocol Solutions

Verdi & VCS

Early RTL Verification

Verdi & VCS

RTL Regression

Virtualizer

Software Bring-up

ZeBu Software

- Single step, full visibility debug for RTL verification
- Full cycle accuracy for performance validation
- Cycle by cycle activity for accurate power estimation

HAPS ProtoCompiler

- Ability to optimize IP and subsystem performance
- Highest performance for SW bring-up on RTL models
- Protocol compliance and certification testing at speed

Power/ Performance Analysis

ZeBu Empower

Platform Architect

Software/ Hardware Validation

HAPS Protocol Interface Card

Speed Adaptor

Compliance/ Certification

HAPS IP Prototyping Kit

Core Technologies: Compile, Debug, Hybrid, Protocols

Synopsys EP-Ready Hardware

Extended

Extended Synopsys **Emulation and Prototyping Ready (EP-Ready) Hardware**

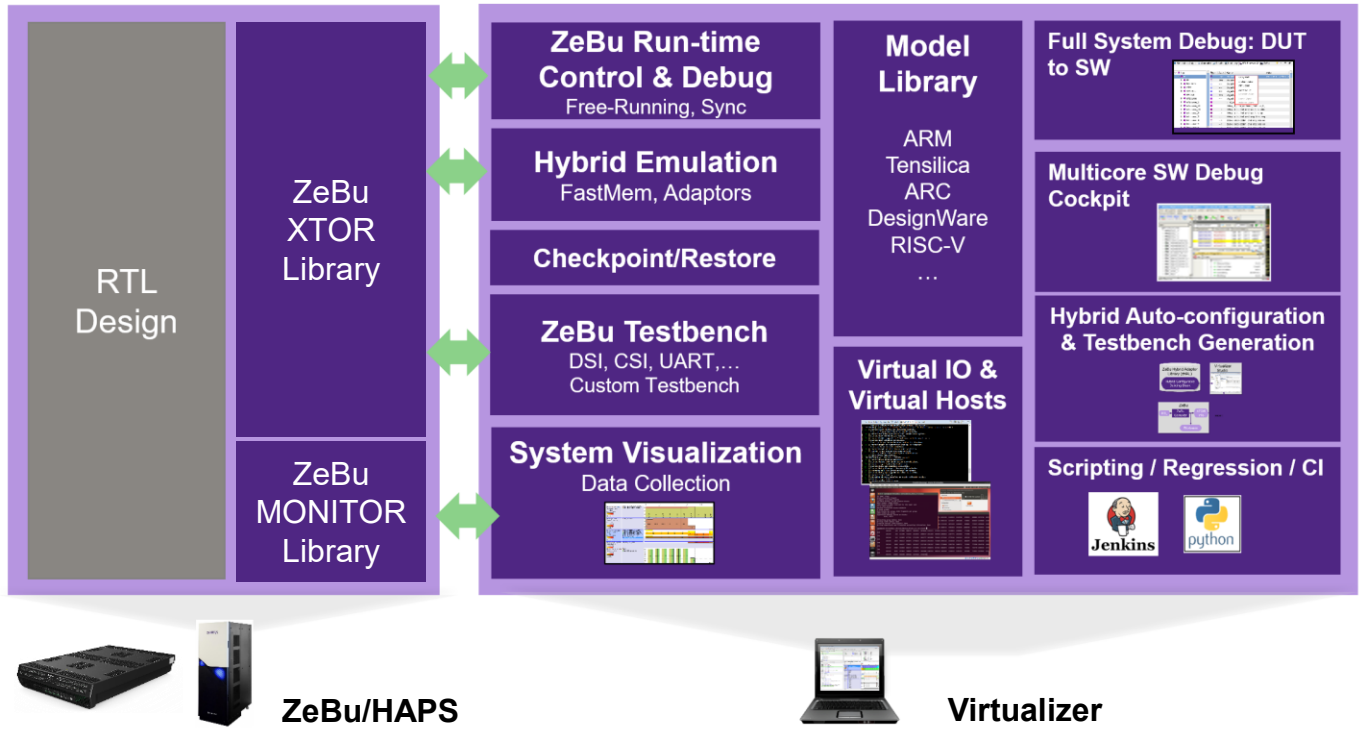
- **One** hardware platform
- **Configurable** for emulation or prototyping
- **Two** software stacks

- **All** emulation and prototyping **use cases**
- Optimize **ROI**
- Get the **most for your budget**
- **Eliminate** the **need to decide balance** of emulation and prototyping hardware up front.

Synopsys Leadership in Hybrid Technologies

Accelerate software bring-up processes with Virtual & Hybrid environments

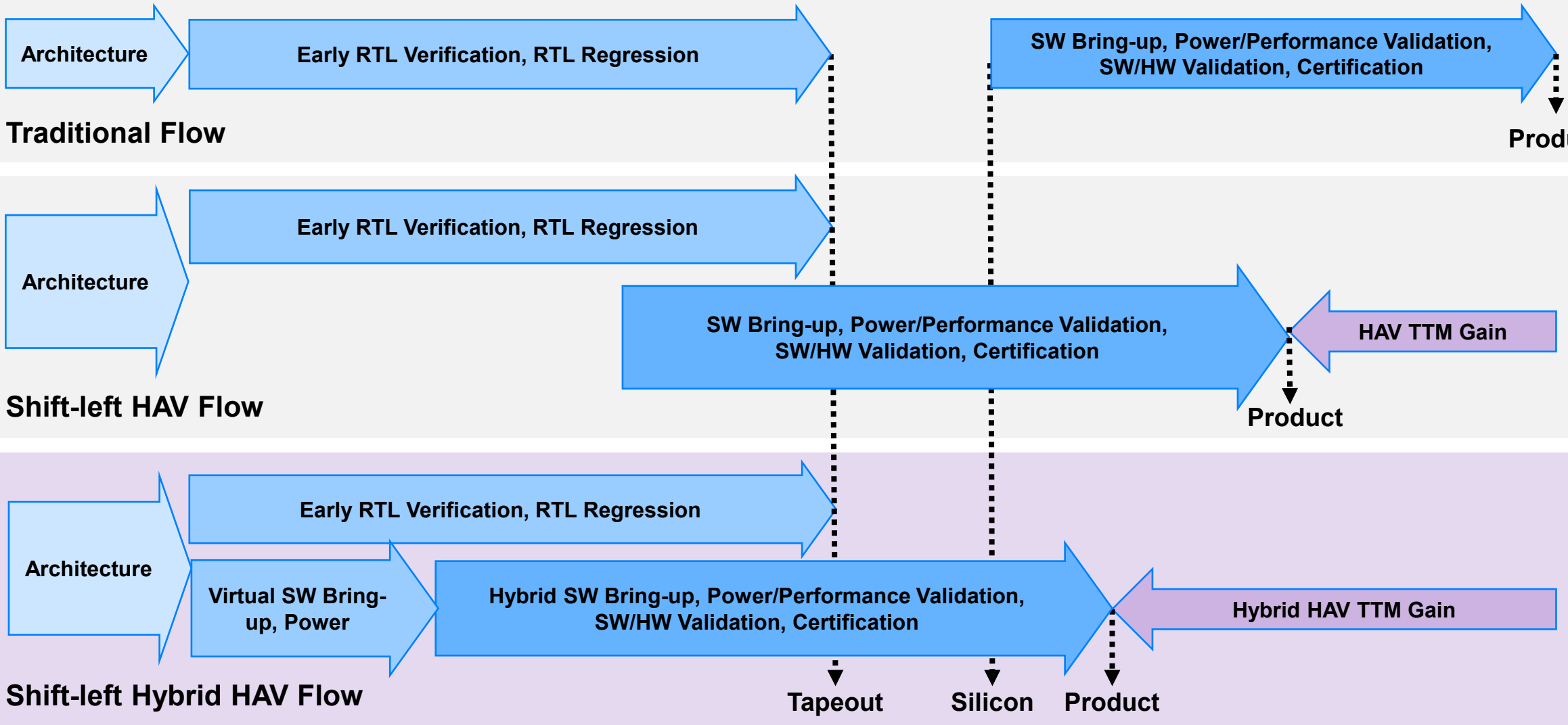
- Combine **virtual models** running on a host server & **HAV system**
- **Complete technology stack**
  - Platform Architect, Virtualizer, ZeBu, HAPS
- **Largest set** of pre-integrated **models**
  - Arm, Tensilica, RISC-V, CEVA & other 3rd party
- Feature **unique technologies**
  - FastMem server, Checkpoint / Restore
- Integrated **System Level Debug**
  - with Software and Hardware debuggers
- **Best productivity** and **performance**
  - Boot Android for Mobile App in under 10 Minutes



"The issue found running SoC software, investigated and narrowed down with ZeBu Hybrid and solved by the design team was really a bug. This would have been a fatal one."

Leading 5G Networking Company

Shift-left with Synopsys Hybrid HAV Solutions



Synopsys Virtual System Adaptors

Host & Devices virtualization for early Software development on ZeBu

Host and Device SW Development

Full-stack SW/Driver/Firmware

Broadest Portfolio

CXL, PCIe, Ethernet, USB, UFS, NVMe

Virtual Network Testing

Ethernet, 5G, Wifi 6

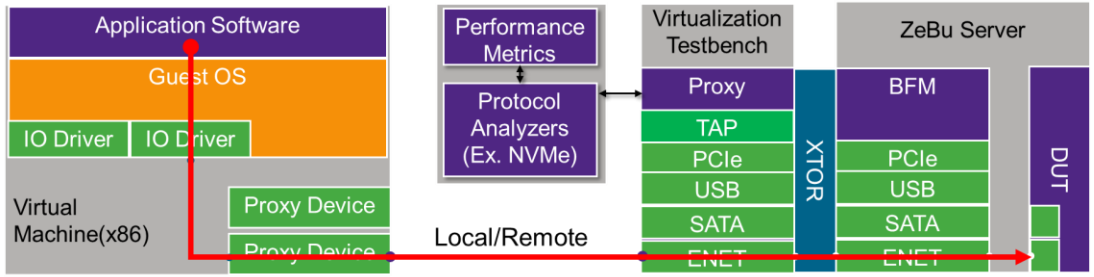
Flexible x86 Platform

Run Any OS – Run from Anywhere

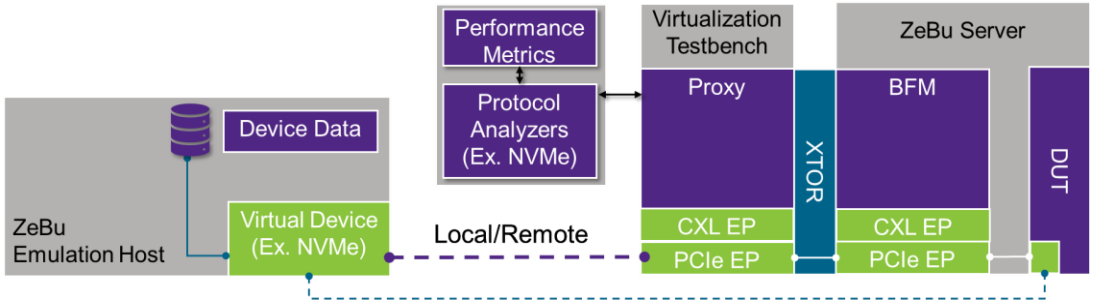
High Performance

Optimized SW and HW architecture

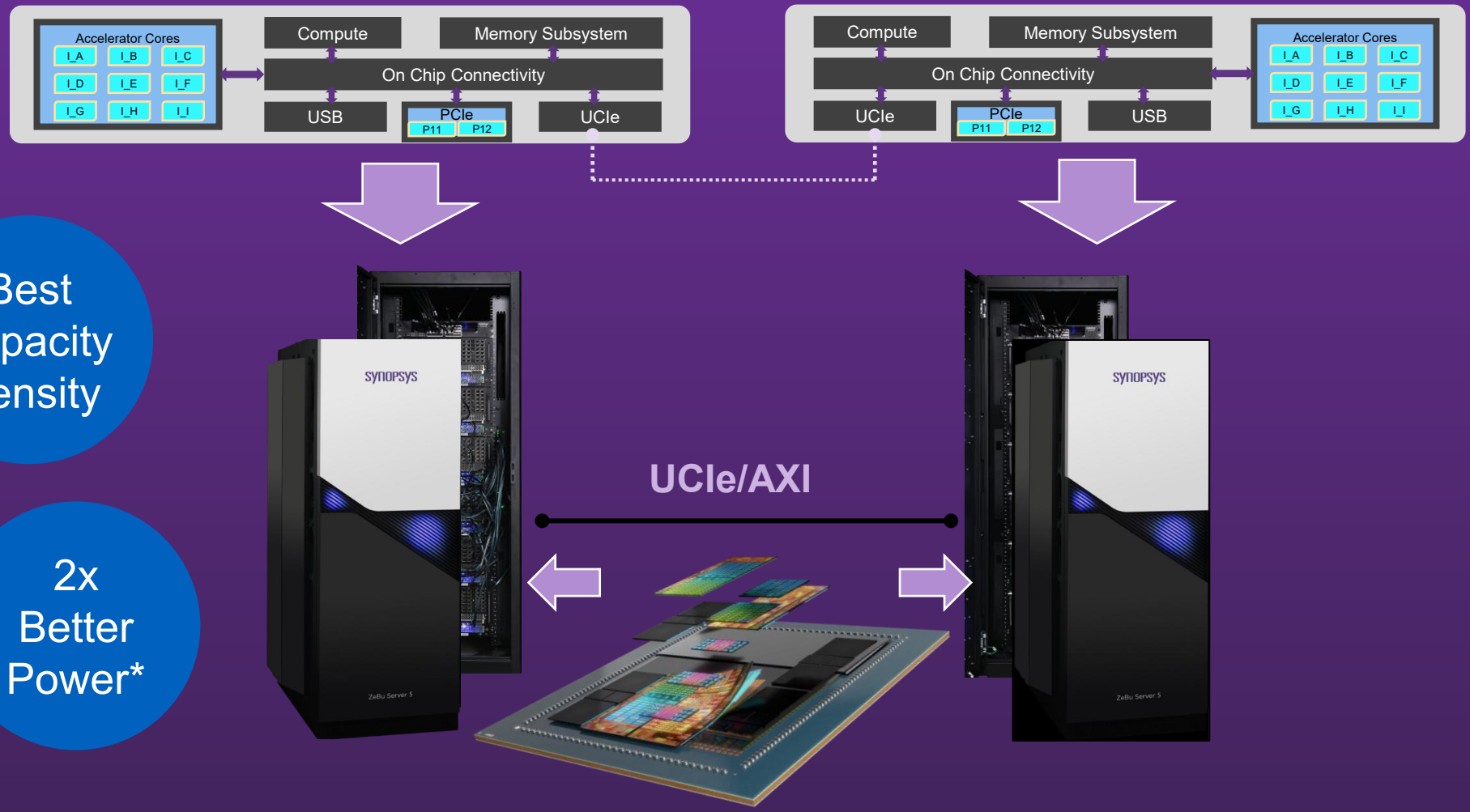
Virtual Host



Virtual Device



Synopsys Modular HAV Methodology
Expanding best TCO



* Versus industry references

ZeBu Empower

Fastest Power Profiling for Real Software Workloads

Key Benefits

Large designs, Realistic workloads, Multiple iterations per day

Actionable power profiling for dynamic and leakage power

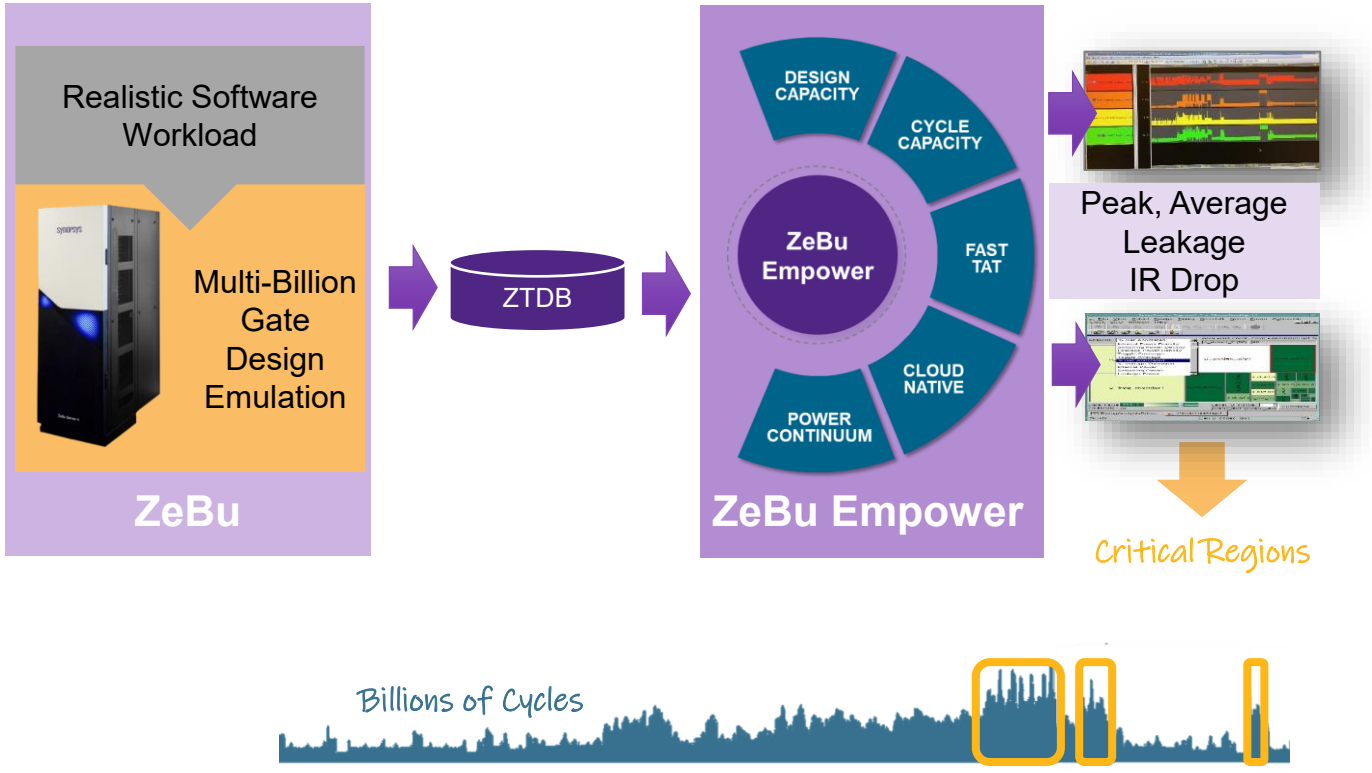
Power critical blocks and vectors feeding into signoff analysis

"ZeBu Empower's impressive performance provides our design teams with a global perspective on power, leading them to the key areas for optimization."

Krishna Rangasayee
Founder and CEO

SiMa.ai

Power Emulation



Hardware and Software Architected for Maximum Compute Throughput

Synopsys Confidential Information

ZeBu Cloud

Flexible Flow Options for SaaS and BYOC

ZeBu Cloud ISO 27001 Certified SOC 2 TYPE I CERTIFIED

SYNOPSYS® FlexEDA/SaaS

SaaS

- ZeBu Compile SW
- Storage for compiled ZeBu Projects

RTL stays in Synopsys Cloud

BYOC*/Home Farm

BYOC

- ZeBu Compile SW
- Storage for compiled ZeBu Projects

Google Cloud aws Azure DATA CENTER

RTL stays in Customer Environment

Secure File Transfer

ZeBu Cloud Datacenter SYNOPSYS®

- ZeBu Environment
- Runtime Host Server
- Compute Server

ZeBu Runtime database; No RTL needed

* BYOC = “Bring-Your-Own-Cloud” means internal Datacenter, GCP, Azure, AWS, “your” internal compute farm.

Recent HAV Customer Success

SNUG Silicon Valley

tenstorrent	rebellions_	arm	Meta
RISC-V debug across simulation and emulation using Virtual JTAG debugger *Real-world use cases with wide spatial coverage*	*Unified development flow for HPC AI achieves* *"SW-before-RTL-freeze"*	*Achieving performance and SW targets for Arm CSS* *Enabling joint ecosystem*	*Rebel AR Glasses* *End-to-end prototyping for entire product functionality*
ZeBu EP	ZeBu Server Virtualizer VCS	ZeBu Server 5	HAPS-100
SNUG SV 2025	SNUG Silicon Valley 2024	SNUG SV 2025	SNUG SV 2025

Expanded Synopsys HAV Product Portfolio

Highest Scalability, **Best Density**

NEW
HAPS-200 & ZeBu-200

Extended
Modular HAV Methodology > 60BG

ZeBu Server 5 | **Extended** Faster Hybrid | ZeBu-200 | HAPS-200 | ZeBu EP | HAPS-100

Highest Performance, **EP-Ready Hardware**

Extended
EP-Ready Hardware

SYNOPSYS®

Thank you