Draft Talk: Design and Verification of Heterogeneous Systems

Speaker:Jebaselvi Johnson, CEO & CTO, Primesoc Technologies LLP

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1. Introduction

Good morning/afternoon distinguished colleagues,
I am Jebaselvi Johnson, CEO and CTO of Primesoc Technologies LLP.
At Primesoc, we specialize in the development of **high-speed digital semiconductor IPs** such as PCIe, CXL, UCIe, and advanced peripheral controllers. Our mission is to enable SoC companies to accelerate their product roadmaps by providing FPGA-proven, production-ready IP blocks.

Today, I will be sharing insights on the **design and verification of heterogeneous systems**, where multiple compute, memory, and connectivity elements come together in a single SoC.

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2. The Rise of Heterogeneous Systems

Modern SoCs are no longer homogeneous compute blocks.
They integrate:

- **Compute clusters** (CPUs, GPUs, AI accelerators, RISC-V cores)
- **High-bandwidth memory systems** (HBM, DDR5, LPDDR5)
- **Standardized interconnects** (PCIe Gen7, CXL 3.0, UCIe)
- **Peripheral subsystems** (MIPI, UART, SPI, I3C, etc.)

This heterogeneity allows systems to achieve performance-per-watt improvements, but it also introduces **significant design and verification complexity**.

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3. Key Design Challenges

- **Protocol Complexity**: Protocols like PCIe Gen7 and CXL 3.0 require strict adherence to layered specifications, link training sequences, and compliance testing.
- **Integration Across Domains**: Connecting compute IPs, memory controllers, and accelerators demands seamless clock domain crossing, reset synchronization, and coherency handling.
- **Scalability**: Next-generation SoCs target multiple nodes (chiplets, 2.5D/3D packaging) with UCIe serving as the standard die-to-die interface.
- **Power Management**: Power intent (UPF/CPF) must be tightly coupled with the IP to enable DVFS, low-power states, and partial shutdowns without breaking coherency.

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4. Verification of Heterogeneous Systems

Verification is the **bottleneck** in heterogeneous SoC design. At Primesoc, we approach this problem through:

1. **Layered Verification Environments**
    - Protocol-specific VIPs for PCIe, CXL, UCIe
    - System-level testbenches for inter-IP coherency validation
2. **FPGA Prototyping**
    - Every IP we ship is **FPGA-proven** before customer delivery
    - Enables early validation of performance and interoperability
3. **Compliance-Centric Testing**
    - Alignment with PCI-SIG, CXL Consortium, UCIe Consortium standards
    - Regression suites built from compliance test cases
4. **Hardware-Software Co-Verification**
    - Providing **reference drivers** and test applications
    - Verifying HW/SW interaction at early stages

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5. Lessons Learned

From our delivery of PCIe Gen6/Gen7, CXL 2.0/3.0, and UCIe 1.x IPs, we have learned:

- Early investment in **CDC/Lint and coding style enforcement** significantly reduces downstream bugs.
- Customers value **integration guides and detailed datasheets** as much as the RTL itself.
- **Scalable verification environments**—capable of moving from IP-level to SoC-level—are essential in heterogeneous designs.

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6. The Road Ahead

Looking forward, we see three trends:

1. **Chiplet-based heterogeneous integration** powered by UCIe.
2. **Unified memory and compute systems** using CXL 3.0.
3. **AI/ML acceleration** driving demand for high-speed interconnect IPs.

At Primesoc, our roadmap includes **USB4.0, Ethernet 800G, HBM, DDR5, and RISC-V controllers**, which will further strengthen the heterogeneous ecosystem.

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7. Conclusion

In conclusion, designing and verifying heterogeneous systems requires not just strong IP, but also robust **integration, verification, and compliance frameworks**.
Primesoc Technologies is committed to being a trusted partner in this journey, offering FPGA-proven IPs that simplify SoC integration for Tier 1 and Tier 2 customers worldwide.

Thank you for your time, and I look forward to further discussions during this conference.